RESUME

Son Van Nguyen, Ph.D.

HOME ADDRESS: 322 Parkview Drive
Schenectady, New York 12303 USA
Phone: (646)-942-6859 (Direct Contact, Mobil)
(518)- 242-3418 (O)
E-mail: SONNGUYEN1@YAHOO.COM ,

BIRTHDATE: 3-18-1956

INTEREST:

Research and development engineering leadership positions in Nano semiconductor technologies and process equipment focusing on Chemical/Physical Vapor Deposition Technology of Dielectrics and Metals.

- Development and Manufacturing: Fabrication and Packaging processing of Nano Electronic and Computer Storage Devices. Nano/micron semiconductor devices: Low K Chemical Vapor.
- Nanofabrication Technologies: Process/Device Integration. Deposition/Etch/Chemical Mechanical Polishing/Lithography Processes:
- Thin Film Storage Technology: Slider, Head and Disk fabrication
- Electronic, Ceramic and Polymeric Materials prepared by Laser and Plasma Assisted Processes for various Microelectronic and Thin Film Storage Applications.
- Physical and Electronic Properties Variations of Materials Properties by Compositional and Bonding Structure Modifications.
- Kinetic Modeling of Plasma and Laser Assisted Processes - Etching and Deposition

EDUCATION:
- Ph.D. in Solid State Chemistry and Physics, January 1981
  Brown University 1978-1981
- National Science Foundation Fellowship - Summer Research
  University of North Carolina at Chapel Hill, 1978
- Bachelor of Art in Chemistry, 1978
  State University of New York at Plattsburgh 1975-1978
- Continuing Education in Electrical Engineering
  Courses: Very Large Scale Integration Technologies, Physics of Field Effect Transistors, Introduction to Complementary Field Effect Transistors, Plasma Science - University of Vermont and IBM Burlington 1982-1984

HONOR & AWARDS:

- IBM First Level Invention Achievement Award, 1988
- IBM Second Level Invention Achievement Award, 1992
- IBM Third Level Invention Achievement Award, 1994
- IBM Fourth Level Invention Achievement Award, 1994
- IBM Fifth Level Invention Achievement Award, 1995
- IBM Sixth Level Invention Achievement Award, 1995
- IBM Seventh Level Invention Achievement Award, 1996
- IBM Eighth Level Invention Achievement Award, 1996
- IBM Ninth Level Invention Achievement Award, 1997
- IBM Tenth Level Invention Achievement Award, 1997
- IBM Eleventh Level Invention Achievement Award, 1998
- IBM Twelfth Level Invention Achievement Award, 1998
- IBM Thirteenth Level Invention Achievement Award, 1999
- IBM Fourteen Level Invention Achievement Award, 2000
- IBM Fifteen Level Invention Achievement Award, 2000
- IBM Sixteen Level Invention Achievement Award, 2001
- IBM Seventeen Level Invention Award, 2002
- IBM Eighteen Level Invention Award, 2004
- IBM Nineteenth Level Invention 2004
- IBM Twentieth Level Invention Award 2005
- IBM Twenty-first Level Invention Award 2005
- IBM Twenty-Second Level Invention Award 2006
- IBM Twenty-Third Level Invention Award 2006
- IBM Twenty-Fourth Level Invention Award 2007
- IBM Twenty-Fifth Level Invention Award 2007
- IBM Twenty-Sixth Level Invention Award 2008
- IBM Twenty-Seventh Level Invention Award 2009
- IBM Twenty-Eight Level Invention Award 2009
- IBM Twenty-Ninth Level Invention Award 2010
- IBM Thirty Level Invention Award 2011
- IBM Thirty First Level Invention Award 2012.
- IBM Thirty Second Level Invention Achievement 2012
- IBM Thirty third Level Invention Achievement Award 2013
- IBM Thirty fourth Level Invention Achievement Award 2013
- IBM Thirty Fifth Level Invention Award 2014
- IBM Thirty Six Level Invention Award 2014
- IBM Thirty Seven Level Invention Award 2014
- IBM Thirty Eight Level Invention Award 2015
- IBM Thirty Nine Level Invention Achievement Award 2015
- **Three Outstanding IBM Technical Achievement Awards 2007, 2010 and 2012 in New Cu- Low k Dielectric Materials Innovation for nano device.**

- **IBM Research Team Extraordinary Accomplishment achievement citation for Cu- Low K Nano Interconnect technology for electronic device manufacturing development 2008.**
- IBM Top Rank Patent Awards.
- IBM Corporate Technical Recognition Awards for most valuable Patents 2004-Flourorinated Oxide Interlevel Dielectric Materials that generated Multimillion dollars Patent Royalty.
Principal IBM Inventor of Flourinated Glass deposition techniques which became the standard of microelectronic industry.
- IBM Corporate Performance Awards (Various Years) –Top Innovator
- Who is Who in America/Who is Who in the East
- Invited Speakers- Material Research Society National Meeting Spring 2008, Spring 2015 San Francisco USA
- Invited Speaker- AMAT Technology Conferences 2013/ IITC 2014
- Invited Speakers: Advanced Metallization Conference 2012, Electrochemical Society Meeting Fall 2008.-Honolulu USA
- Section Chairman of Plasma Deposition: 7th International Symposium in Plasma Chemistry,. Eindhoven, Netherlands. 1985
- Chairman of IBM 1985 Plasma Symposium. Burlington, VT 1985
- Invited Panel session discussion member on Novel Deposition . US National Science Foundation Task Force on "Engineering and Research Needs for Electronic Material Processing". University of Delaware, Newark, DE June 1985.
- Invited Speaker. Semiconductor West 1995 Technical Seminars
- Invited Speaker. International Conference on Metallurgical Coating and Thin Films. San Diego, USA 4/1994 and 5/1995.
- Invited Plenary Speaker. Fourth International Symposium in Plasma Etching and Deposition for Microelectronic Application. Paris, France. November 1985.
- Invited Speaker. American Vacuum Society National Meeting. Houston, Texas. November 1985.
- Invited Speaker. SEMICON EAST. Boston, Massachusetts. 1984
- Invited Speaker. New England Chapter, American Vacuum Society. New Bedford, Massachusetts. September 1984.
- Invited Speakers at University of Vermont, State University of New York, Florida State University, University of North Carolina, University of Wisconsin at Madison, Penn State. 1985-1996
- Exxon Research Fellow 1980 - 1981.
- Honor Graduate. State University of New York, 1978.
- National Science Foundation Summer Research Fellowship.1978

RESEARCH & TEACHING EXPERIENCE:

- RESEARCH STAFF- (Senior MEMBER & group leader) : 11/2006-Present
  Dielectrics and Exploratory Materials, **IBM at Albany Nanotech Center**
  Albany, University at Albany, Albany, New York 12203

Exploratory Research in Nanotechnology for Nano Device Fabrication in Sub-20 nm Nanodevices: Plasma assisted Atomic Layer Deposition. Nano Interconnect Technology. Low k Dielectrics material for Cu Interconnect for 32/22 nm CMOS devices. Metal Cap and liners for nano device BEOL Interconnect. 3-D

Device packaging process and integration. .Carbon nanotube interconnect Back End of the Line for Future Nano devices. **Principal Dielectric CVD scientist/engineer for IBM at Albany Nanotech University at Albany for Cu Bilayer Low k Cap (k~3.8) and metal cap and ULK (k~2.2-2.7) film/process technology implemented into 45/32/22/14/10/7 nm Interconnect for IBM semiconductor Alliance** . We achieved Team Extraordinary Accomplishment achievement award at IBM Research for Cu-Low K Nano Interconnect technology.
Extensive Mentoring and Teaching of graduate students and new hires

- RESEARCH STAFF- MEMBER: May 2003- September 2006
  Dielectrics and Exploratory Materials, IBM Thomas Watson Research Center
  Yorktown Heights, New York USA
  Accomplishment: Exploratory Stable low k (k<3.0) dielectric for advanced semiconductor device fabrication. Development of advanced Ultra low-k CVD SiCOH dielectrics (k=2.0-3.0) with low lost and improved mechanical and electrical properties for 300 mm Fabrication Line. Developed advanced processes for low k (2.7-2.4) CVD SiCOH films and established Cu/low k integration suitable for 65-22 nm CMOS electronic devices. **Principal research scientist/engineer for the Development and implementation of nano porous SiCOH Dielectric with K~2.7 into 45/32/22 nm CMOS device manufacturing for IBM Semiconductor Technology Alliance (IBM-Sony-Toshiba-AMD-Chatered-Samsung-Infineon) on Semiconductor Technology Development.** -

- CHIEF TECHNOLOGY OFFICER, Low-K Dielectric Group: July 02- May 03
  Applied Materials Inc., Santa Clara, CA 95054 USA
  Job Description: Responsible for Technology R&D of low-K dielectrics suitable for <0.10 um high performance electronic devices.
  Accomplishment: Developed key technologies & direction for CVD low-K, received several key US patents (8) for various CVD low-k/Cu .
  Develop Integrated Plasma CVD/E-Beam low K (k < 2.7) system.

.

* SENIOR SCIENTIST/ENGINEER. July 1999-July 2002
  IBM Corporation. IBM Almaden Research Center, San Jose, CA 95120
  Job Description: Develop Reactive Ion Etching, Ion Milling for sub-0.1 um Semiconductor and Magnetic Recording Head Fabrication . Plasma CVD/Etching Fabrication Process for Storage Devices. Low Dielectric Constant Material and Metal Etching, low and high dielectric constant and Insulating Materials Deposition.
  Accomplishment: Developed 0.1-0.15 micron high (>10:1) Aspect ratio polymeric structure suitable for advanced Cu, NiFe, Al/Ag metal wiring structures by etching or plating for advanced electric and storage devices. Patterning processes for advance Spin valve and Magnetic DRAM devices.
* SENIOR SCIENTIST/ENGINEER . JUNE 1996-July 1999
  IBM Corporation. IBM System Storage Division, San Jose, CA 95193
  Job Description: Air Bearing Slider Technology Development, Advanced Slider- RIE Processing, Ion Milling, Solid

State Lubrication Films, Cleaning.:
Advanced Plasma process technology. Plasma
Abatement of Chlorofluorocarbon to minimize environmental
Green-house effect. Laser micro machining of advanced MR/GMR
slider devices
Accomplishment: Developed CFC Plasma Abatement Technology
for IBM SSD for worldwide installation. Laser Corner
Rounding Technology Development. Advanced RIE Etch Processes
for Slider Air Bearing Surface Patterning. Advanced plasma
Carbon and F-Cx for Slider Overcoat and slider Lubrication.

* SENIOR ENGINEER. MAY 1994- JUNE 1996
IBM Corporation. IBM Microelectronics, Hopewell Junction, NY 12533
Job Description: Insulator Technology Development for sub-
Quarter micron (0.25-0.15 um) DRAM (256M & 1Giga bits) and
Sub-quarter micron future CMOS devices. Low dielectric
Constant materials: process technology development
Advanced tooling and process development. Principal Engineer
For Advanced CVD/RIE process technology development for IBM
Advanced Semiconductor R&D Center.
Accomplishment: Developed new F-Oxide and low-k (HSQ) high density
Plasma films for sub-quarter micron IC at IBM ASTC.
Established High density Plasma CVD capability at IBM ASTC
And advanced low temperature CVD Oxide. Sub-quarter micron
Stack capacitor. **Principal IBM Inventor of Flourinated Glass deposition techniques that became the standard of microelectronic industry**.

* ADVISORY ENGINEER. JULY,1992-1994
IBM Corporation. IBM Microelectronics, Hopewell Junction, NY 12533

Job Description: Insulator Technology Development for sub-
Quarter micron (0.18-0.25 micron) DRAM (256M-1 Gigabits).
Advanced insulator development for future CMOS devices.
Electron Cyclotron Resonance and Magnetically Enhanced Plasma
Processing. Clustered and Integrated Multi-step Processing
with advanced tooling (AME5000, 5500, ECR CVD
Novellus Concept 1 , HDP CVD system, Lam Integrity).
Accomplishment: Established processes for 256 Mbit Insulator
deposition: low temperature CVD processes including doped and
undoped oxides, and other advanced insulator CVD. Exploring/
Developing Processes for advanced CMOS technology including
High Density Plasma CVD, LPCVD BPSG, Fluorinated Oxide and
Sub-atmospheric CVD TEOS/O3.
Middle of The Line/M0 Integration/Process development:
Inter-metal Gate conductor Fill with SACVD TEOS/O3, LPCVD BPSG.
Improved M0 Damascene Process to meet 256 Mbit DRAM requirement-
. BEOL Process developments for both 256M and 1Gbit DRAM

* ADVISORY ENGINEER. FEBRUARY, 1989- JULY 1992
IBM Corporation. General Technology Division, Essex Junction, VT 05452

Job Description: Plasma Dry Process Development for
sub-half micron (0.18-0.35 micron) DRAM (64-256M-1Gbits).
Electron Cyclotron Resonance and Magnetically Enhanced Plasma
Processing. Clustered and Integrated Multi-step-Processing
with advanced tooling (AME5000).
Accomplishment: **Plasma CVD Fluorinated Silicon Oxide**
Developed sub-half micron dry etch process
for doped PolySilicon, Metal Silicide gate stack conductors
for early T0 phase of 64 Mbit DRAM . Module development for
Trench Recess I & II for T0 64 Mbit and 256 Mbit DRAM.
Process Technology: Evaluated and Developed Conformal
step coverage Plasma and Thermal CVD TEOS and Silane Oxide
Process suitable for 64-256 Mbits DRAM technology. Developed
New PECVD Processes for Fluorinated Oxide ,BN, SiBN,
Fluorinated Nitride
, Plasma Oxidation Process with Ozone result in
several patent applications. Stack and Trench Capacitors
Developments for 0.25 micron CMOS Technology. Thin Insulator
(3-10 nm) Oxide/Nitride/Oxide Developed for 256 Mbit DRAM.
High dielectric Constant Ta_2O_5 Development for Future Device

* Staff Engineer and Project Leader. March 1987- Feb. 1988
IBM Corporation. General Products Division
San Jose, California 95193. Job Descriptions : Advanced
Surface Treatment Process Development for Thin Film Disks,
Alternative Overcoats for Thin Films Disk, Lubrication
Process Development, Surface Bonding Enhancement.
Plasma Dry Processing for Alternative Thin Film Disks
Overcoat and Surface Texture Patterning.
Accomplishments: Developed Alternative Dipping Lubrication
Process for Thin Films Disks. Successfully Researched and
Developed Dipping Lubrication Process to a Stage that
it become a Plan-of-record for Thin Film Disks Project
in only 3 months. Scaled up process and trained engineers
and technicians for Pilot line Production
Current Scaled up Process is being used in Thin Film
Disk Manufacturing at IBM San Jose.
IMPORTANT PUBLICATION RELATED TO PROJECT : TECHNICAL
REPORT TR 02.1464:
" Dipping Process Development of Perfluorocarbon Lubricant Coating
for Thin-Film Astro Disks", Son Van Nguyen, E. Yang and R. Kulkani
May 1988, IBM Confidential Restricted.

* Staff Engineer . July, 1984 - February, 1987.
IBM Corporation. General Technology Division.
Essex Junction, Vermont 05452.

Teaching Experience: Thesis Advisor for Graduate student thesis research at IBM in University - Industry Research Program (IBM - Clarkson University). 1985 - 1986.
Student Thesis: Excimer Laser Etching of Polysilicon Film

- Supervised Summer Co-op students at IBM .1984-1985
- Instructor for IBM Graduate level course: "Plasma Processing for Microelectronic Applications". 1985 .
- Work Experience: Plasma Processing for Microelectronic Applications: Etching and Deposition. Low Pressure Chemical Vapor Deposition, Sub-micron Lithography, Thin Dielectric Materials, Laser Etching of Semiconducting and Insulating Silicon, Polymer and Conducting Metallic Films. Physical Analysis and Electrical Characterization of Thin Film Materials: Amorphous Silicon, Silicon Nitride, Oxide, Oxynitride, Metal (W, Co, WSix) and Organosilicon Polymer. Kinetic Modeling of Laser and Plasma Assisted Process. Accomplishments: Established Significant Visibility of Plasma Deposition and Etching in Burlington. Assisting Plasma Process Development for Megabits Chips. Researched and Developed 2% Silane Plasma Deposition to substitute for 100 % Silane Process. Identified, Developed and Established Laser Etching Technology in IBM Burlington and Showed That This Technology is Unsuitable for Silicon Processing.

* Senior Associate Engineer. Work experience : Plasma Science Tool Optimization, Characterization of Polymer and Thin Dielectric deposited by Plasma Process. 1981 - 1984.
  IBM, Essex Junction, Vermont 05452.
  Accomplishments : Installed Plasma Enhanced Deposition Tools, Developed Plasma Silicon Nitride, Silicon Oxide and Oxynitride Deposition Processes Suitable for various Silicon Integrated Circuit Fabrication Processes. Researched and Developed Various Plasma Enhanced Chemical Vapor Deposition Processes for Many Types of OrganoSilicon Polymers. Dry Etching Process Development.

* Research Chemist. Work experience: Synthetic Fuel Research-Coal Gasification and Liquidification Catalysis. .Summer 1980.
  Exxon Research and Engineering Company, Baytown, Texas 77520
  Accomplishments: Developed New Magnetic Measurement Methods to Study and Monitor the Activity of Catalysts During Various Stages of Coal Gasification and Liquidification Process. This resulted in a research grant from Exxon to Brown University for the continuation of this work.

* Teaching and Research Assistant. Research Experience: Photovoltaic properties of transition metal oxide - Synthesis, characterization by X-ray powder diffraction, Fourier Transform Infrared, measuring photoelectronic and Electrical properties, Thermogravimetric analysis, magnetic

Measurement.
Correlation between magnetic and crystallographic properties of transition metals supported on amorphous carbon - effect of catalytic properties of metals under various process conditions. Works sponsored by Exxon Research and Engineering Company at Brown University.
Teaching Experience: General, Inorganic and Physical Chemistries: Laboratory and Courses. 1978 - 1981.
Brown University, Providence, Rhode Island 02912.

* Research Assistant. Research in Inorganic Synthesis of Promising Superconducting Materials. Summer 1978.University of North Carolina at Chapel Hill, North Carolina 27514

* Teaching and Research Assistant. Research in Organic Synthesis, Computer Simulation of Chemical Reactions.
Teaching Assistant - General and Physical Chemistry 1976-78
Chemistry Department, State University of New York at Plattsburgh, New York 12901.

EXTERNAL PUBLICATIONS & PRESENTATIONS:

* Over 100 US Patents issued and filed

* Over 100 External Technical Publications and Presentations.

A- REFEREED JOURNAL & BOOK ARTICLES

a) **THESIS RESEARCH**

1) "Preparation and Photoelectronic Properties of Cd_2GeO_4 ".
S.V. Nguyen, R. Kershaw, K. Dwight and A. Wold, Material Research Bulletin, V. 14, pp. 1535-1539 (1979).
2) "Preparation and Photoelectronic Properties of the System $Cd_2Ge_{1-x}Si_xO_4$"; S.V. Nguyen, R. Kershaw and A. Wold, Journal of Solid State Chemistry, February 1981.
3) "The Crystallographic and Magnetic Properties of Dispersed Nickel Particles on Amorphous Carbon support"; S.V. Nguyen, Ph.D. Thesis, Brown University, April 1981.

b) Plasma & Laser Processing, Material Science, Kinetic , semiconductor technology, Micro and nanoelectric devices, Nanoscience, Magnetic computer storage

4) "The Initial Transient Phenomena in Plasma Enhanced Chemical Vapor Deposition Process". S.V. Nguyen, P.Pan, Applied Physics Letters, v.45(2), pp.134-136(1984).
5) "The Variation of Physical Properties of Plasma deposited Silicon Nitride and Oxynitride with Their Compositions". S.V. Nguyen, P. Pan, S. Burton, J. of Electrochemical Society, V.131, pp.2348-2353(1984).

6) " Plasma deposited Organosilicon Polymers - Deposition, Characterization and Application in Multilayer Resist Lithography". S.V.Nguyen, J. Underhill, S. Fridmann and P.Pan; published in Journal of The Electrochem. Soc., V.132, pp.1925-1932(1985).
7) " Variation of Hydrogen Bonding, Depth Profiles and Spin Density of Plasma Deposited Silicon Nitride and Oxynitride with Deposition Mechanism". S.V. Nguyen, W. Lanford and A.L. Rieger. Published in Journal of The Electrochemical Society, V.133, pp. 970-975 (1986).
8) " Plasma Assisted Chemical Vapor Deposition Thin Films for Microelectronic Applications". S.V. Nguyen, appeared in Journal of Vacuum Science and Technology B4(5), pp. 1159-1167, Sept./Oct. 1986
9) " The Bonding Structure and Compositional Analysis of Plasma Enhanced and Low Pressure Chemical Vapor Deposited Silicon Nitride and Oxynitride Films". S.V.Nguyen, S. Fridmann, J. Abernathy and M. Gibson. Published in a book: "Emerging Semiconductor Technology ", Editor : D. Gupsta ,American Society for Testing and Material, Material, V. STP 960, pp. 173-189 (1987).
10) " Plasma Enhanced Chemical Vapor Deposition ". S.V. Nguyen, Book Chapter # 4, pp. 112-141," Handbook of Thin Film Deposition Processes and Techniques", Editor: K. Schuegraf, Noyes Publications USA, 1988.
11) " Plasma deposition and Characterization of Thin Si-rich Silicon Nitride Films". S.V. Nguyen and S. Fridmann, Journal of Electrochem. Society, V. 134, No# 9, pp.2324-2329 (1987).
12) "Effect of Si-H and N-H Bonds on Electrical Properties of Plasma Deposited Silicon Nitride and Oxynitride Films". S. V. Nguyen Journal of Electronic Materials, V. 16, No#4, pp.275-281 (1987).
13) "Excimer Laser Assited Etching of Polysilicon Films"; Son Van Nguyen, S. V. Nguyen, M. Armacost and J. Rembetski, Journal of Mater. Research, V.2(6), pp. 895-901, Nov./Dec. 1987 .
14) " The characterization of Electron Cyclotron Resonance Plasma Deposited Nitride and Oxide Films", S. V. Nguyen and K. Albaugh, J. of Electrochem. Soc., V. 136(10), pp. 2835-2840(1989).
15) " Magnetically Enhanced Reactive Ion Etching of Poly Gate Electrode Smaller than 0.5 micron ", S. V. Nguyen, D. Harmon and D. Dobuzinsky .Solid State Technology, pp. 73-77, October 1990.
16) " Reaction Mechanism of Plasma and Thermally Assisted Chemical Vapor Deposition Process of Tetraorthosilicate Oxide Films", S. V. Nguyen, D. Harmon, D. Dobuzinsky, S. Fridmann, R. Gleason. J. of Electrochemical Society, V. 137, No.7, pp.2209-2215 (1990).
17) " Plasma Deposition and Characterization of High Quality Silicon Oxide Films", S. V. Nguyen, D. Dobuzinsky, S. Fridmann, R. Gleason and M. Gibson. Thin Solid Films, V.193/194, pp.595-609(1990).
18) "Substrate Trenching Mechanism in Plasma and Magnetically Enhanced Reactive Ion Etching of Polysilicon Gate Electrode", S. V. Nguyen, D. Dobuzinsky, G. Chrisman and S. Stiffler. J. of Electrochem. Soc., V. 138, No.4, pp. 1112-1117 (1991).
19) "A new leakage Mechanism in sub-5nm Oxynitride dielectric", T. Nguyen, Son V. Nguyen, D. Dobuzinsky , D. Carl and J. Korejwa. Applied Physic Letter, V.63(14), pp. 1972-1974, October 1993.
20) " Evidence of p-n junction formation in plasma CVD BN deposition

on silicon", T. Nguyen, S. V. Nguyen and D. Dobuzinsky. Applied Physic Letter, V.63(15), pp.2103-2105, 1993 .

21) " Plasma deposition and characterization of Boron Nitride Films", S. Nguyen, T. Nguyen, H. Treichel and O. Spindler. J. of Electrochem. Soc, V.141, N0#6, pp. 1633-1638 (1994)

22) " High Selectivity Magnetically Enhanced Reactive Ions Etching of Boron Nitride", D. Cote, S. Nguyen, D. Dobuzinsky, C. Basa and R. Neureither. J. of Electrochem. Soc., Vol. 141, pp.3456-3462(1994).

23) " Novel Fingered Stack Capacitor ", S. Nguyen, Tue Nguyen, D. Carl and D. Dobuzinsky. J. Electrochem. Soc., V.142, pp.L111-113(1995)

24) " Low temperature Chemical Vapor Deposition Processes and Dielectrics for for Microelectronic circuit manufacturing at IBM", D.R. Cote, S. V. Nguyen, W.J. Cote, S. L. Pennington, A. Stamper and D. V. Podlesnik IBM Journal of Research and Development, V.39, pp.437-464 (1995).

25) " Advanced Metallization Technology for 256Mbit DRAM", P. Kucher, H. Aochi, J. Gambino, T. Licata, T. Matsuda, S. Nguyen, M. Okazaki, H. Palm, M. Roney, Applied Surface Science, V. 91, pp.359-366(1995)

26) " CVD of Fluorosilicate Glass for ULSI applications", M. J. Shapiro, S. V. Nguyen, T. Matsuda, D. Dobuzinsky, Thin Solid Films, pp.503-507 V.270, December 1995.

27) " Fluorine Diffusion from Fluorosilicate Glass", M. J. Shapiro, T. Matsuda, Son V. Nguyen, C. Park and C. Dziobkowski, J. of Electrochem. Soc., pp. L156-L158, V.143, No#7 (1996).

28) " Ultrathin RTP Oxynitride dielectric on Planar, Trench and 3-D Structures", S. Nguyen, T. Nguyen, D. Carl, D. Pricer, D. J. Korejwa and D. Dobuzinsky. Microelectronics and Reliability, V.1, pp.81-85 (1998).

29) " Modulation-Doped Silicate Glass", M. Ilg, Son Van Nguyen, K.Uram, M. Kraxenberger, N. Sander, C. Park, Supperlattices and Microstructures, Vol. 24, No#5, pp.385-388 (1998)

30) " High Density Plasma Chemical Vapor Deposition of Silicon-Based Dielectrics for Microelectronic Fabrication", Son Van Nguyen, IBM Journal of Research and Development,V.43, No#1/2,pp.109-126(1999).

31) " Plasma-Assisted Chemical Vapor Deposition of Dielectrics", D. R. Cote, Son Van Nguyen, A. K. Stamper, D. Armburst, D. T. Tobben, R. Conti, and G. Y. Lee, IBM Journal of Research and Development, V.43, No#1/2, pp.5-38(1999).

32) " Titanium carbide Etching in High Density Plasma", R. Hsiao, D. Miller, A. Kellock; Applied Surface Science, V.148, pp.1-8,(1999).

33) “ E-Beam Writing: A Next Generation Lithography (NGL) Approach for Thin Film Head Critical Features”, R.E. Fontana, J. Katine, M. Rooks, R. Wiswanathan, J. Lille, S. MacDonald, E. Kratschmer, C. Tsang, Son Van. Nguyen, N. Robertson, P. Kasiraj. , IEEE Trans.Magnetics, V.38, N0.1, pp. 95-100 (2002)

34) " Etch of Spin Valve Capping Layers for Sensor Stabilization Applications" W. P. Jayasekara, S. Zhang, D. Mauri, S. Nguyen, T. Shatz, IEEE Trans. Magnetics September 2003

35) "Ultrathin (5-35 nm) SiCNH Dielectrics for Damascene Cu Cap Application: Thickness Scaling and Oxidation Barrier Performance Limitation", Son Nguyen, Thomas Haigh Jr., Thomas Shaw, Steven Molis, Chet Dziobkowski, C. Zahakos, Steve Cohen, Hosadurga Shobha, E. Liniger, C. K. Hu, Griselda Bonilla, Nancy Klymko, and Alfred Grill, Electrochemical Society Transactions: Issue Title: Processing, Materials, and Integration of Damascene and 3D Interconnects, Volume: 33, Issue: 12, pp.137-145 (2010) .

36) " In Situ Co/SiC(N,N) Capping Layers for Cu/Low-k Interconnect, C.C.Yang, B. Li, H. Shobha, S. Nguyen, A. Grill, J. Aubuchon, M. Shek and D. Edelstein, IEEE Electron Device Letter, Vol 33, No, 4, pp.588-560 (2012)

37) " Robust ultrathin (20-25 nm) trilayer dielectric low k Cu damascene cap forsub-30 nm nanoelectronic devices." , Son Nguyen, T. Haigh Jr., M. Tagami , A Grill, S. Cohen, H. Shobha, C. Hu, E. Adams , E. Linigger , T. Shaw , T. Cheng , H. Yusuf, Y. Xu, T. .Ko, S. Molis, T. Spooner, S. Skodas , X. Liu,, G. Bonilla, D. Edelstein. Electrochemical Society Transactions: Issue Title: ULSI Cu Interconnects Technology (2012). ECS Transactions. 01/2012; 41(43):3-9

38) "Progress in the Development and Understanding of Advanced Low k Dielectrics films for VLSI Interconnects – State of the Art"; Al Grill, Steve Gate, SON NGUYEN, E. , D. Priyadarshin; Appl. Phys. Rev. 1, 011306 (2014); http://dx.doi.org/10.1063/1.4861876.

38a) Linking strain anisotropy and plasticity in copper metallization Conal E. Murray, Jean Jordan-Sweet, Deepika Priyadarshini, and Son Nguyen, APPLIED PHYSICS LETTERS 106, 181902 (2015). [http://dx.doi.org/10.1063/1.4919788]

REFEREED PROCEEDING VOLUMES and EXTERNAL PRESENTATIONS

39) "Plasma Deposition of Silicon Nitride and Oxynitride Films Using Inert Carrier Gases as Transport Agents".S.V. Nguyen, Proceeding of Symposia on Thin Nitride Insulating Films, pp. 453-459, v.83-8(1983). The Electrochemical Society. Presented at The Electrochemical Society Spring 1983 Meeting, San Francisco USA.

40) "Optical Emission Spectroscopic Study of Silicon Nitride and Oxynitride Deposition Glow Discharge". S.V. Nguyen, Proceeding of 9th International Conference on Chemical Vapor Deposition, pp.213-232,

V.84-6(1984), the Electrochemical Society. Presented at ECS meeting Spring 1984, Cincinnati, Ohio USA.

41) "Infrared, Auger and Electrical Characterization of Plasma deposited Silicon Nitride and Oxynitride Films". S.V. Nguyen, Extended Abstract pp.25-26, presented at the 1983 Electronic Material Conference, Burlington, Vermont USA.

42) "The Kinetic Model of Penning Reactions in Plasma Deposition of Silicon Nitride and Oxynitride". S.V. Nguyen, Invited paper presented at New England American Vacuum Society, Sept. 26,1984 Boston Meeting.

43) " A review of Fundamental Aspects of Plasma Deposition"; S.V.Nguyen, Invited Paper, SEMICON EAST, September 1984, Boston USA.

44) " Plasma deposited Organosilicon Polymers - Deposition, Characteriza -tion and Application in Multi-layer Resist Lithography". S.V.Nguyen, J. Underhill, S. Fridmann and P.Pan; Presented and published in the Proceed. of Fifth Plasma Processing Symposium of the Electrochemical Society,pp.535-536, October 1984, New Orlean, USA.

45) "Silicon Oxynitride Films as Intermediate Layer in a 3-layer Resist System for Sub-micron Lithography". J. Underhill, S.V. Nguyen, M. Kerbaugh, D. Sundling; Proceed. of Photo-Optical Instrumentation Engineers (SPIES), V.539, pp.83-89(1985).

46) "The Role of Hydrogen Bonding on Metal-Nitride-Semiconductor (MIS) Electrical Properties of Plasma Deposited Silicon Nitride and Oxynitride Films". S.V. Nguyen, Extended Abstract pp.52-55,1985 Electronic Material Conference, Boulder, Colorado USA.

47) "Novel Deposition Processes for Electronic Material Processing - Issues in Plasma Deposition for Microelectronic". S.V. Nguyen, Invited Presentation in National Science Foundation Workshop on Engineering Needs in Electronic Processing. Appeared in Executive Summaries of the workshop pp. C1-C10 ; June 1985, University of Delaware, Newark, Delaware, USA.

48) " Variation of Hydrogen Bonding, Depth Profiles and Spin Density of Plasma Deposited Silicon Nitride and Oxynitride with Deposition Mechanism". S.V. Nguyen, W. Lanford and A.L. Rieger. Presented and appeared in Proceed. of Seventh International Symposium in Plasma Chemistry, V.1, pp.56-61(1985), Eindhoven, The Netherland.

49) " Hydrogen Diffusion Between Plasma Deposited Silicon Nitride/ Aluminum interfaces under Plasma Processing and Its Effect on Field Effect Transistor Device Threshold Voltage (V¢t!) Shift". S.V. Nguyen and S.U. Kim, Extended Abstract # 228, pp.437-438(1985), Fall 1985 Electrochemical Society Meeting, Las Vegas, Nevada. Full paper appeared in Proceed. of Reduced Temperature Processing for VLSI , pp.533-544, V. 86-5, Electrochem. Soc. 1986.

50)" Plasma Enhanced Chemical Vapor Deposition : Fundamentals and Applications to Microelectronic". S.V. Nguyen, Invited paper No# VMTuA1, Extended Abstract, p.73; American Vacuum Society 1985 National Meeting, Houston, Texas USA.

51) Plenary Lecture :"Fundamental Aspects of Plasma Deposition for Microelectronic Applications". S.V. Nguyen, Proceed. of Third International Symposium on Plasma Etching and Deposition for Microelectronic, pp.223-232, the French and International Societies

for Vacuum Science and Technology, Paris, France November 1985.

52) " The Bonding Structure and Compositional Analysis of Plasma Enhanced and Low Pressure Chemical Vapor Deposited Silicon Nitride and Oxynitride Films". S.V.Nguyen, S. Fridmann, J. Abernathy and M. Gibson. Presented at the Fourth International Symposium on Semiconductor Processing, San Jose, California USA; January 1986.

53) " Plasma deposition and Characterization of Thin Si-rich Silicon Nitride Films". S.V. Nguyen and S. Fridmann, presented at the Fall 1986 Electrochemical Society, San Diego, California; Extended Abstract # 322, pp.483-484. Full paper published in The Electrochemical Society Volume 87-6 : PLASMA PROCESSING, pp.564-581 (1987). Editors: G.S. Mathad, R. A. Gottscho and G. C. Schwartz.

54) " Reactive Ion Etching of insitu-doped Polysilicon films using $CCl_2F_2 + NH_3$ Plasma". S.V.Nguyen, D. Dobuzinsky, F. White and M. Kerbaugh; presented at the 1986 Electrochemical Society Meeting in San Diego, California, Extended Abstract # 312, pp. 467-468. Full paper published in Proceeding of 6th Plasma Processing Volume 87-6 : PLASMA PROCESSING, pp.552-564 (1987). Editors : G.S. Mathad, R. A. Gottscho and G. C. Schwartz.

55) " Plasma Deposited Organosilicon Polymers " Seminar presented at Department of Chemistry, State University of New York at Plattsburgh, Febuary 1986.

56)" 193 nm ArF Excimer Laser Etching of Polysilicon film"; M. Armacost, S.V. Babu, S.V. Nguyen and J. Rembetski; Paper presented in Material Research Society, December 1986 Meeting, Boston, Massachusett and appeared in Material Research Society Symposia Proceeding: " Science and Technology of MicroFabrication ", V.76, pp. 147-156 (1985); Editors: R. E. Howard et. al.

57) " Plasma deposited Silicon Nitride and Oxynitride "; Invited talk at University of North Carolina at Charlotte and Microelectronic Center of North Carolina; October 16,1986.

58) " 193 nm ArF Excimer Laser Assisted Etching of Polysilicon using Cl_2 "; Son Van Nguyen, S. Fridmann and J. Rembetski, presented at Fall 1987 Material Research Society Meeting in Boston. Abstract B4-11, page 119. Full paper published in Material Research Society Volume 101, pp. 33-40 (1988). Editors: D. Ehrlich et al.

59) " Hydrogen Diffusion Between Plasma Deposited Silicon Nitride-Polyimide interfaces"; Son Van Nguyen, M. Kerbaugh, presented at Fall 1987 Material Research Society Meeting in Boston. Abstract I4-3, page 274. Full paper published in Material Research Society Volume 101, pp. 247-256 (1988). Editors : R. Jaccodine et al.

60) " The Characterization of Electron Cyclotron Resonance Plasma Deposited Nitride and Oxide Films", S. V. Nguyen and K. Albaugh, presented in Electrochemical Society Fall 1988 meeting, PP.437-438, Proceeding Volume#88-2.

61) " Magnetically Enhanced Reactive Ion Etching of Sub-half Micron Polysilicon Gate Electrodes ", S. V. Nguyen, D. Harmon and D. Dobuzinsky. Presented in the Second International Symposium on ULSI, Los Angles, CA 1989. Full paper published in Electrochem. Soc. Proceed. Vol.#89-9, pp.474-485(1989). Editor: C. M. Osburn.

62) " Reaction Mechanisms of Plasma and Thermally Assisted Chemical Vapor Deposition Process of Tetraorthosilicate Oxide Films", S. V. Nguyen, D. Harmon, D. Dobuzinsky, S. Fridmann, B. Gleason. presented at the 9th International Symposium in Plasma Chemistry. Pugnochiuso, Italy 1989. Full paper published in Proceed. Vol.#II, pp.1134-1139(1989) by Inter. Union of Pure and Applied Chemistries.

63) " Plasma Deposition and Characterization of High Quality Silicon Oxide Films", S. V. Nguyen, D. Dobuzinsky, S. Fridmann, R. Gleason and M. Gibson. Presented in the 8th International Symposium in Thin Films, April 1-6, 1990, San Diego, California.

64) "Substrate Trenching Mechanism In Plasma and Magnitically Enhanced Reactive Ion Etching of Polysilicon Gate Electrode", S. V. Nguyen, D. Dobuzinsky, G. Chrisman and S. Stiffler. Presented in Electrochemically Society Spring 1990 Meeting in Montreal, Canada

65) "Plasma and Magnitically Enhanced Reactive Ion Etching and Trenching Mechanism of Polysilicon Gate Electrode", S. V. Nguyen, D. Dobuzinsky, G. Chrisman and S. Stiffler. Invited Paper Presented At University of Wisconsin at Madison, NSF Center For Plasma-Aided Engineering. December 15, 1989.

66) "Initial Transient Phenomena in Plasma deposition of silicon oxide films ", S. Nguyen, D. Dopp, D. Dobuzinsky and M. Gibson. Presented at Fall Electrochemical Society meeting in Seattle, 1990. Full paper published in Proceed. of 11th Interna. CVD conference, pp.404-409 (1990)

67) "Kinetic and Characterization of Thin Oxide (4-6 nm) film grown using low temperature plasma-enhanced processing with nitrous oxide" T. Nguyen, S. Nguyen, and D. Dobuzinsky. Presented at The Fall Electrochemical Society meeting in Seattle, 1990, Abstract # 318, pp. 462-463. 1990 Conference Proceeding.

68) "Evidence of Oscillating surface reaction during Plasma Oxidation of Silicon with Oxygen". Son Nguyen, T. Nguyen, D. Dobuzinsky, R. Gleason and M. Gibson. Presented at Material Research Society Spring 1991 Meeting, paper # E6.2, Anaheim, California. Full published in MRS Symposium Proceeding Vol. 223, pp. 229-234 (1991).

69) "High Quality Thin (3-6 nm) Oxide films formation by Ozone Plasma Oxidation". Son Nguyen, T. Nguyen, D. Dobuzinsky, R. Gleason and M. Gibson. Proceed. of the 180th Electrochemical Society Fall 1991, pp. 209-110, Phoenix, Arizona

70) "From Keyboard desktop to talking Computer, from Mega to Gigabit Chip, From Micro to Nano-fabrication : A Material Sciences Approach" Invited Seminar, University of Vermont, Burlington, USA. 12/6/1992.

71) " Plasma Deposition and Characterization of Fluorinated Silicon Nitride". Son Nguyen, D. Dobuzinsky, R. Gleason and M. Gibson, Proced. of the 181th Electrochemical Society Spring 1992 Meeting, p. 209-110, St. Louis, Missouri, USA.

72) " Plasma Deposition and Characterization of Boron Nitride Films " Son Nguyen, T. Nguyen, H. Treichel and O. Spindlers. Presented at International Conference of Metallurgical Thin Films, April 1993.

73) " Plasma Deposition and Characterization of Silicon Doped Boron Nitride Films ".Son Nguyen, T. Nguyen, H. Treichel and

O. Spindlers. Presented at International Symposium in Plasma Chemistry 8/22-27/1993 Loughborough, England and published in ISPC Proceeding Volume 3, pp.981-986, Edited by John Harry International Union of Pure and Applied Chemistry.

74) " Magnetically Enhanced Reactive Ion Etching of Boron Nitride", D. Cote, Son Nguyen, D. Dobuzinsky, K. Basa and R. Neureither. Presented at SPIE Conference, 9/1993. Monterey, California USA

75) " Advanced CVD processes and dielectrics for sub-half micron microelectronic fabrication", S. Nguyen and T. Matsuda, Invited paper, abstract# TC2.01, p.A173 Invited paper presented at 1994 International Conference on Metallurgical Coating & Thin Films. San Diego, April 1994.

76) " BPSG Insulator for sub-half micron trench fill ", S. Nguyen, D. Cote, D. Dobuzinsky, K. Uram, N. Sander and R. Shugrue, paper # 251, pp. 406-407, Proceeding Volume 94-1.Spring 1994 Electrochem Meeting, San Francisco, May 1994.

77) " Dual Frequency Plasma CVD Fluorosilicate Glass Water Absorption and Stability", Mike Shapiro, Tetsuo Matsuda and S. V. Nguyen, presented at and published in Proceeding of the First Dielectric for ULSI International Conference (DUMIC), pp.118-123(1995). Santa Clara, California.Febuary 1995

78) " Dual Frequency Plasma CVD Fluorosilicate Glass for 0.25 um ILD" Tetsuo Matsuda, Mike Shapiro and S. V. Nguyen, presented at and published in Proceeding of the First Dielectric for ULSI International Conference (DUMIC), pp.22-28(1995). Santa Clara, California.Febuary 1995

79) " Fluorosilicate Glass for ULSI ILD", Mike Shapiro, S. V. Nguyen, and Tetsuo Matsuda. Invited paper presented at the 1995 International Conference on Thin Films San Diego, April 1995.

80) " Advanced Metallization Technology for 256 Mbit DRAM"; P. Kuecher T. Licata, M. Roney, M. Okazaki, S. NGUYEN, T. Matsuda and H. Aochi, presented at Materials for Advanced Metallization '95 European Workshop, Radebeul, Germany, March 19-22, 1995.

81) " Plasma Deposition Chemistry of Fluorinated Silicon Oxide Films" S. Nguyen, M. J. Shapiro, T. Matsuda, D. Dobuzinsky and C. T. Dziobkowski, presented at and published in The Proceeding (Vol. 4) of 12th International Symposium in Plasma Chemistry, pp. 1975-1980 Editors: J. V. Heberlein, D. W. Ernie and J. T. Robert, IUPAC, Minneapolis, Minnesota, USA. August 21-25, 1995

82) " The Characterization of High Density Plasma CVD Silicon Oxide Films for 0.25 um ULSI", S. Nguyen, G. Freeman, D. Dobuzinsky, K. Kelleher, R. Nowak, T. Sahin, D. Witty. Present at and published in, Proceeding of 12 th International VLSI Multilevel Interconnect Conference, pp.69-75, June 1995

83) " Ultrathin RTP Oxynitride dielectric on Planar, Trench and 3-D Structures", S. Nguyen, T. Nguyen, D. Carl, D. Pricer, D. J. Korejwa and D. Dobuzinsky. Presented and published at Proceeding of 25 th European Solid State Device Research Conference, pp.251-254, The Hague, the Netherland, September 1995

84) " CVD of Fluorosilicate Glass-The Role of Fluorine". Mike Shapiro,

S. V. Nguyen, T. Matsuda, C. Park, C. T. Dziobkowski and D. Dobuzinsky. Invited paper presented at the 1995 Semicon West. July 1995 San Francisco.

85) " The Characterization of High Density Plasma CVD Silicon Oxide Films for 0.25 um ULSI", S. Nguyen, G. Freeman, D. Dobuzinsky, K. Kelleher, R. Nowak, T. Sahin, D. Witty. Invited paper to Applied Material Technical Seminar at the 1995 Semicon West. July 1995 San Francis

86) " BPSG Insulator for sub-half micron CMOS Device ", S. Nguyen, D. Cote, D. Dobuzinsky, K. Uram, N. Sander and R. Shugrue, Invited paper to Lam Research Material Technical Seminar at the 1995 Semicon West. July 1995 San Francisco.

87) Invited Seminar: "High Density Plasma CVD Silicon Oxide for ULSI Fabrication", Penn State University, January 29, 1996

88) "Water Absorption Study of HDP CVD Silicon Oxide Films", N. Shoda, P. Weigand, T. Matsuda, S. NGUYEN, M. Shapiro, J. Rzuczek, T. Jones, presented at and published in the Second Dielectric for ULSI International Conference (DUMIC) Proceeding Volume pp. 13-20, Santa Clara, California.Febuary 1996

89) "Advanced LPCVD BPSG deposition process for sub-0.25 micron microelectronic fabrication", M. Ilg, M. Kirchhoff, S. Nguyen, presented at Electrochemical Society Spring 1996 Meeting Proceeding abstract # 760, p.941. Full paper appeared in ECS Publication PV96-5 Proceeding of 13 th International Conference on CVD, pp.860-865, Edited by T.M. Bessmann, M. D. Allendorf, Mc.D. Robinson and R. Ulrich.

90) " CVD and Characterization of Fluorosilicate Glass", Mike Shapiro, T. Matsuda ,S. V. Nguyen, C. Park and Chet Dziobowski, presented at Electrochemical Society Spring 1996 Meeting Proceeding abstract # 764, p.947. Full paper appeared in ECS Publication PV96-5 Proceeding of 13 th International Conference on CVD, pp.850-855, Edited by T.M. Bessmann, M. D. Allendorf, Mc.D. Robinson and R. Ulrich.

91) "Process-Induced Gate Oxide Damage Issues in Advanced CVD Processes" D. Cote, Son Nguyen, V. McGahay, C. Waskiwicz, S. Chang, A. Stamper, P. Weigand, N. Shoda and T. Matsuda, presented at and published in Proceeding Volume of 1st International Conference in Plasma Process-Induced Damage, pp.61-66, May 13-14, 1996. Santa Clara, California.

92) "HDP CVD Silicon Oxide Deposition: The effect of Sputtering on Film Properties", P. Wiegand, N. Shoda, T. Matsuda, S. NGUYEN, M. Shapiro, J. Rzuczek, M. J. Shapiro, T. Jones and R.Ploessi, Proceding of the 13th International VLSI Multilevel Interconnect Conference (VMIC),pp.75-80, Santa Clara, CA, USA.June 18-21, 1996

93) "Integration of Dielectrics for 0.25 micron Metallization Level: HDP-CVD vs SA-CVD", P. Wiegand, H.Palm , S. NGUYEN and E. Kiewra, Proceeding of the 14th International VLSI Multilevel Interconnect Conference (VMIC),pp.565-570,Santa Clara, CA, USA. June 10-12, 1997.

94) " High Density Plasma Deposition and Characterization of F-Oxide Films". Son Van Nguyen, P. Weigand, J. Rzuzeck, M. J. Shapiro, and C. T. Dziobkowski, presented at and published in The Proceeding (Vol. 3) of 13th International Symposium in Plasma Chemistry, pp. 1153-1158 Editors: J. V. Heberlein, D. W. Ernie and J. T. Robert, IUPAC, Bejing, China, August 18-22, 1997

95) " Hydrogen Content and Permeability of Thin CVD Silicon Nitride and Oxynitride Layer", M. Kirchoff, D. Cote, M. Hauf, S. Nguyen, and W. Hoesler, Proceedings of the 192th Meeting, The Electrochemical Society, The 14th International Symposium on Chemical Vapor Deposition, Paris, France, pp.1230-1237(1997).

96) " The Role of Inert Carrier Gases in Reactive Ion Etching of Al2O3-TiC (N58) Mixed Phases for Slider Air Bearing Surface Patterning" S. V. Nguyen, D. Perez, R. Craig, M. Straub, A. Ting, R. Hsiao, C. Hwang, D.Haney and T. Neumann, Proceeding of the 194th Meeting of the Electrochemical Society Meeting Abstract# 511, Boston USA, 1998

97) "Point of Use High Density Plasma Abatement of Perfluorinated Global Warming Reactive Ion Etching Gases in Slider Fabrication" Son V. Nguyen, S. Wyatt, M. Singh, M. Moreno, A. Ting, R. Jewett and C. Camus, Proceeding of the 14th International Symposium in Plasma Chemistry,pp.2545-2550,V.5, Praha, Czech Republic, 8/1999.

98) "High Density Plasma Abatement of Perfluorinated compounds used in Slider Fabrication"; Son Van Nguyen, R. Jewett, S. Wyatt, M. Singh, M. Moreno, A. Ting, and C. Camus; 2000 Semiconductor FAB TECH.

99) " Topography Evolution of High Aspect Ratio sub-micro photo resist trench structure by High Density Plasma", Son Van Nguyen, Quang Le, J. Latimer, P. Rice; 15th International Symposium in Plasma Chemistry Proceeding, , July 9-13, 2001, Orlean, France

100) " Low temperature High density plasma deposited Fluorocarbon films and surface modification method to reduce surface energy", Son Van Nguyen, Richard Hsiao, R. Stover, D. Pocker, Andrew Ting, P. Chen, C. Hwang .15th International Symposium in Plasma Chemistry , July 9-13, 2001, Orlean, France

101)" E-Beam Writing: A Next Generation Lithography (NGL) Approach for Thin Film Head Critical Features", R.E. Fontana, J. Katine, M. Rooks, R. Wiswanathan, J. Lille, S. MacDonald, E. Kratschmer, C. Tsang, Son Van. Nguyen, N. Robertson, P. Kasiraj. Paper C6, The Magnetic Recording Conference, August 2001,

102)"High Aspect Ratio Sub-Micron Copper Coil Fabrication with Novel Image Transfer Plasma Etching Processing", **S. Nguyen**, Q. Le, P. Kasiraj, D. Tang and J. Latimer, Electrochemical Society Fall 2002 Meeting, Salt Lake City , Utah, USA

103)" Etching of Spin Valve Capping Layers for Sensor Stabilization Application W. P. Jayasekara, S. Zhang, D. Mauri, **S. Nguyen**, T. Shatz, A. J. Devasahayam and J. Wang, IEEE 2003 Intermag Conference Proceeding, Boston, USA, April 2003

104) Reliability, Yield, and Performance of a 90 nm Cu/SiCOH BEOL Technology, D. Edelstein*, C. Davis, L. Clevenger, M. Yoon, H. Rathore, A. Cowley, T. Nogami[1], B. Agarwala, S. Arai[2], A. Carbone, K. Chanda, S. Cohen, W. Cote, M. Cullinan, T.

Dalton, S. Das, P. Davis, J. Demarest, D. Dunn, C. Dziobkowski, R. Filippi, J. Fitzsimmons, P. Flaitz, S. Gates, J. Gill, A. Grill, D. Hawken, K. Ida[1], D. Klaus, N. Klymko, M. Lane, S. Lane, S. Law[4], J. Lee, W. Landers, W-K. Li, Y-H. Lin, E. Liniger, H. Liu[4], W. Liu[4], X-H. Liu, A. Madan, S. Malhotra, J. Martin[3], S. Molis, C. Muzzy, D. Nguyen, **S. Nguyen**, M. Ono[2], C. Parks, D. Questad, D. Restaino, A. Sakamoto[1], T. Shaw, Y. Shimooka[2], A. Simon, E. Simonyi, J. Tan[4], S. Tempest, T. Van Kleeck, S. Vogt, Y-Y. Wang, W. Wille, J. Wright, C-C. Yang, and T. Ivers, IITC 2004 Meeting Proceeding, p.214, San Francisco, California June 7-9, 2004

105) COMPREHENSIVE RELIABILITY EVALUATION OF A 90 nm CMOS TECHNOLOGY WITH Cu/PECVD LOW-k BEOL—D. Edelstein, H. Rathore, C. Davis, L. Clevenger, A. Cowley, T. Nogami, B. Agarwala, S. Arai, A. Carbone, K. Chanda, S. Cohen, W. Cote, M. Cullinan, T. Dalton, S. Das, P. Davis, J. Demarest, D. Dunn, C. Dziobkowski, R. Filippi, J. Fitzsimmons, P. Flaitz, S. Gates, J. Gill, A. Grill, K. Ida, D. Klaus, N. Klymko, M. Lane, S. Lane, J. Lee, W. Landers, WK. Li, Y-H. Lin, E. Liniger, X-H. Liu, A. Madan, S. Malhotra, J. Martin, S. Molis, C. Muzzy, D. Nguyen, **S. Nguyen**, M. Ono, C. Parks, D. Questad, D. Restaino, A. Sakamoto, T. Shaw, Y. Shimooka, A. Simon, E. Simonyi, A. Swift, T. Van Kleeck, S.Vogt, W. Wille, J. Wright, C-C. Yang, M. Yoon, and T. Ivers,, IEEE Proceeding International Reliability Physics Symposium (IRPS), p. 18 , Phoenix Arizona , April 25-29, 2004.

106) BEOL Integration with Cu/SiCOH (k~2.8) low k Interconnect at 65 nm Ground Rule,

M. Fukasawa, S. Lane, M. Angyal, K. Chanda, F.Chen, C. Christiansen, J. Fitzsimmons, J. Gill, K. Ida, K. Inouue, K. Kumar, B. Li, P. Laughlin, I. Mlville, M. Miami, S. Nguyen, C. Penny,. C. Sakamoto, Y. Shimooka, M.Ono, D. Mcherron, T. Nogami and T. Ivers, International Interconnect Conference, 2005 Meeting Proceeding, p. , San Francisco, California June 6-8, 2005103).

107) K. Ida, **Son Van Nguyen**, ... Et al. .. " Low k (~2.7) Dielectric SiCOH Film Development and Integration for 65 nm CMOS Devices", Proceedings of Advanced Metallization Conference 2005 , (AMC Conference , September 28-30, 2005, Colorado Spring, CO USA

108). M. Fukasawa, ..., **S. Nguyen**,... Et al. , " BEOL Process Integration with Cu/SiCOH (k=2.8) Low-k Interconnects at 65 nm Groundrules", Proceedings IITC 2005, IEEE International. Interconnect Technol. Conference, June , 2005, Burlingame, CA and Japan Advanced Metallization Conferences, Oct 12-14, 2005 Tokyo Japan

109) Sarah Lane, ..., S. Nguyen .... Et al., " BEOL Process Integration with Cu/SiCOH (k=2.8) Low-k Interconnects at 65 nm Groundrules", Invited Paper: Japan Advanced Metallization Conferences, Oct 12-14, Tokyo Japan

110) T. Nogami , S. Nguyen, ... Et al. , " Low k SiCOH Integration for 65 nm BEOL Groundrules", Invited Paper: VMIC Conference Sept 2005, Santa Clara

111) " 65nm Cu Integration and Interconnect Reliability in Low Stress K=2.75 SiCOH" McGahay, G. Bonilla, F. Chen, C. Christiansen, S. Cohen, M. Cullinan-Scholl, J. Demarest, D. Dunn, B. Engel, J.A. Fitzsimmons, J. Gill, S. Grunow, B. Herbst, H. Hichri, K. Ida*, N. Klymko, M. Kiene**, C. Labelle**, T. Lee, E. Liniger, X.H. Liu, A. Madan, K. Malone, J. Martin**, P.V. McLaughlin, M. Minami*, S. Molis, C. Muzzy, S. Nguyen, J.C. Patel, D. Restaino, A. Sakamoto*, T.M Shaw, Y. Shimooka***, H. Shobha, E. Simonyi, J. Widodo#, A. Grill, R. Hannon, M. Lane, H. Nye, T. Spooner, R. Wisnieff, and T. Ivers , International Interconnect Conference, 2006 Meeting Proceeding, , San Francisco, California June 5-7, 2006

112) "Low and ultralow-k dielectrics for high performance interconnects.", A. Grill,

, V.Patel, S. Gates, S. Nguyen, C. Dimitrakopoulos and D. Restaino, Invited Paper , International Conference on Silicon Technology for ULSI and TFT, Italy, July 2007

113) "Enhanced Cracking Resistance of Plasma Deposited Low k SiCOH Films with Nano Imbedded Layers Insertion" Son. Nguyen*, E. Liniger*, K. Ida[1], B. Herbst*, K. Malone, N. Klymko, S. Cohen*, E. Simonyi*, S. Lane, C. Dziobkowski, M. Lane*, A. Grill*, D. Restaino, S. Gates*, D. Edelstein*, T. Nogami* , Tom Ivers; Electrochemical Socity Meeting Proceeding, May 6-10, 2007 , Chicago , USA

114) " Plasma Deposited Low k SiCOH Films with improved properties using Nano Imbedded Layers Insertion" Son. Nguyen*, E. Liniger*, K. Ida[1], B. Herbst*, K. Malone, N. Klymko, S. Cohen*, E. Simonyi*, S. Lane, C. Dziobkowski, M. Lane*, A. Grill*, D. Restaino, S. Gates*, D. Edelstein*, Tom Ivers; **Invited Paper**. Proceeding of Vietnam First Workshop on Nanotech , p299-301, November 15-17, 2007 , Vung Tau, Vietnam

115) " Advanced Low k Cap Dielectric Materials for Highly Reliable Ultra Large Scale Integration Devices" , Son Nguyen et al., **Invited Paper**: Material Research Society, Spring 2008, San Francisco, California USA, March 2008

116) "Lightly Porous SiCOH 2.7 Dielectric Film Development for 65/45/32 nm Advanced Nanoelectronic CMOS Devices" by S. Nguyen, V. McGahay, M. Sherwood, N. Klymko, S. Cohen, E. Simonyi, A. Grill, H. Shobha, D. Restaino, S. Lane, S. Molis, K. Malone, E. Liniger, V. Patel, S. Gates, D. Edelstein, S. Mehta and T. Ivers ; **Invited Paper** : The Electrochemical society Fall 2008 Meeting, Honolulu, Hawaii USA. October 2008

117) " Advanced Bilayer low-K Dielectric Cap for Reliable High Performance Cu-Low-k Interconnect in ULSI Devices", G. Bonnilla, L.A. Clevenger, C. K. Hu, **Son Nguyen**, T. Cheng , H. Shobha, Z. Sun, S. Cohen, A. Fisher, K. Chanda, E. Liniger, W.P. Liu, Y. Xu, J. Gill, T. Shaw, M. Chase, S. Molis, R. Quon, , Advanced Metallization Conference, pp. 673-679,San Diego, California USA , October 2008

118) " Plasma deposition and development of ultra low k bilayer SiCx/SiCNy dielectric Cu cap for nanoelectronic CMOS BEOL", **Son Nguyen** et al., The Electrochemical Society Fall 2009 Meeting, paper# 2159 Vienna, Austria , 2009.

119)" A Back End of Line Structures with Ultra low k material (k<=2.4), J. Bao, N. Lustig, E. Engbrecht, J. Gill, R. Filippi, T.C. Lee, K. Chanda, D. Kioussis, A. Lisi, T. Cheng, S.B. Law, A. Simon, P. Flaitz, J. Choi, W. Tseng, E. Zielinski, S.M. Gates, A. Grile, **Son Nguyen**, H. Shobha; International Interconnect Technology Conference 2010 Proceeding Volume, paper 4.5, San Francico, California ,June 6-9, 2010.

120) "Ultrathin (5-35 nm) SiCNH Dielectrics for Damascene Cu Cap Application: Thickness Scaling and Oxidation Barrier Performance Limitation. ",**Son Nguyen**, T. Haigh Jr., T. Shaw, S. Molis, C. Dziobkowski, C. Zahakos, S. Cohen, H. Shobha, E. Liniger, C. K. Hu, G. Bonilla , N. Klymko, A. Grill. The Electrochemical Society Fall 2010 meeting, paper # 1685, Las Vegas, Nevada USA October 10-15, 2010.

121) "High Reliability and Low Resistance CuMn Damascene Interconnection for 32nm-node BEOL and its Extendibility to 22nm and beyond " ;T. Nogami, T. Bolom, A. Simon, B-Y. Kim, C-K. Hu, K. Tsumura, A. Madan, P. Flaitz, C. Parks, P. DeHaven, R. Davis, M. Zaitz, B. St. Lawrence, R. Murphy, L. Tai, S. Molis, S-H. Rhee, T. Usui, C. Cabral Jr., J. Maniscalco, L. Clevenger, B. Li, C. Christiansen, F. Chen, T. Lee, J. Schmatz, H. Shobha, F. Ito, T. Ryan, **Son Nguyen**, D. Canaperi, J. Arnold, S. Choi, S. Cohen, E. Liniger, H-C. Chen, S-T. Chen, T. Vo, J. Kelly, O. Straten, C. Penny, G. Bonilla, P. Kozlowski, J. Wynne, T. Spooner, and D. Edelstein· International Electron Device Meeing 2010 Conference, Paper Abstract # 33.5 December 6-8,2010, San Francisco, CA USA.

122) " Low-k and Ultralow-k Dielectrics for VLSI Interconnects: State of the Art"**,** Alfred Grill, Steve Gates, E. Todd Ryan and Son Nguyen, Proceeding of Electrochemical Society Spring 2011 Meeting, Abstract #1404, Montreal, Canada.

123) " Robust Ultrathin (20-25 nm) Trilayer dielectric low k cu Damascene Cap for nono BEOL Cu interconnect", Son Nguyen, T. Haigh Jr., A. Grill, H. Shobha, S. Cohen, ….et al., Proceeding of Electrochemical Society Fall 2011 Meeting, Abstract #1933, Boston, USA. Oct 9-15,2011.

124) "Ultralow-k PECVD pSiCOH dielectrics and their implementation in VLSI interconnects"., A. Grill, S. Gate, E.T. Ryan and Son Nguyen, American Vacuum Society 2011 Meeting, Abstract Book, paper EM-WeM3, p. 137. Nashville, Tennessee, USA Oct 30-Nov 3, 2011.

125)"Novel ultralow-k interconnect dielectric fabricated with single precursor" , Son Nguyen, Hosadurga Shobha, Stephan Cohen1, Anita Madan, Eduard Adams, Kumar Virwani, Donald Canaperi, Todd Ryan, Alfred Grill; Material Research Society Spring 2012 Meeting, April 9-13,2012 San Francisco, California. USA

126) " *In Situ* Co/SiC(N,H) Capping Layers for Cu/Low-*k* Interconnects", C.-C. Yang, B. Li, H. Shobha, S. Nguyen, A. Grill, W. Ye, J. AuBuchon, M. Shek, and D. Edelstein, 2012 IEEE International Interconnect Technology Conference, June 4-7, San Francisco, California

127) " Advanced Cap for Copper Low K Interconnects " **,** **Son Nguyen** et al., **Invited Paper**, Advanced Metallization Conference, October 9-11, 2012, Albany NANOTECH Center, University at Albany New York USA.

128) "Time Dependent Dielectric Breakdown Extendibility of Ultralow k Materials to 14nm BEOL and Beyond " , Eric Liniger,.. **Son Nguyen** et al., **Invited Paper**, Advanced Metallization Conference, October 9-11, 2012, Albany NANOTECH Center, University at Albany New York USA

129) "Caps for Copper Low K Interconnects " , **Son V. Nguyen**, A. Grill, H. Shobha, T. Haigh, Jr., D. Priyadarshini, C.-C. Yang, C.-K. Hu, T. Cheng, T. Ko, S. Cohen, E. Liniger, Y. Xu, T. Shaw, E. Adams, A. Madan, N. Klymko, C. Parks, S.-T. Chen, J. Chen, S. Molis, A. Simon, G. Bonilla, ,D. Edelstein, D. Canaperi, T. Spooner, D. Kioussis, Y. Lin , M. Tagami, L.-Q. Xia, S. Reiter, M. Balseanu, and M.Shek, Material Research Society , Spring 2013, San Francisco, California USA.

130) " Electromigration Comparison of Selective CVD Cobalt cap with PVD TiN and CVD Co liner on 22 nm- Groundrule Dual-Damascene Cu Interconnect" , A. Simon, T Bolom, … , **Son Nguyen**,… J Aubuchon; IEEE International Reliability Physics Society Meeting, April 14-18, 2013 Monterey, California USA.

131) "Selective deposition of advanced ultrathin nano layers selective Cobalt and conformal SiN conformal caps for sub-20 nm Copper/Low k interconnects" , Son V. Nguyen, H. Shobha, D. Priyadarshini, C.-C. Yang, T. Haigh Jr., C.-K. Hu†, S. Cohen, E. Liniger, T. Shaw, E. Adams J. Burnham, T. Ko, Y. Lin, A. Madan, N. Klymko, C. Parks, D. Yang, Jr., S. Knupp, S. Molis, A. Simon, G. Bonilla, A. Grill, D. Edelstein, D. Canaperi, T. Spooner, D. Collin, L.-Q. Xia, S. Reiter, M. Balseanu, and M.Shek, Applied Materials Electronic Technology Conference on Selective Deposition and Removal of Materials, Monterey, California, USA June 4-6, 2013

132) "Advanced ultrathin nano layers selective Cobalt and conformal SiN conformal caps for sub-20 nm Copper/Low k interconnects" , Son V. Nguyen, H. Shobha, D. Priyadarshini, C.-C. Yang, T. Haigh Jr., C.-K. Hu†, S. Cohen, E. Liniger, T. Shaw, E. Adams J. Burnham, T. Ko, Y. Lin, A. Madan, N. Klymko, C. Parks, D. Yang, Jr., S. Knupp, S. Molis, A. Simon, G. Bonilla, A. Grill, D. Edelstein, D. Canaperi, T. Spooner, D. Collin, L.-Q. Xia, S. Reiter, M. Balseanu, and M.Shek, 2013 International Conference on Atomic Layer Deposition Proceeding volume pp 124-125. , Section B-Selective ALD, July 29-31, 2013 San Diego, California USA.

. 133) "Integrated In-situ Selective Co and Conformal SiN Dielectric Barrier Cap for Cu/low k Interconnects**"**   ; Deepika Priyadarshini, SON. NGUYEN, H. Shobha, S. Cohen, T. Shaw, E. Liniger, C.K. Hu, C. Parks, E. Adams, J. Burnham, G. Bonilla, A. Grill, D. Canaperi, D. Edelstein, D. Collins, M. Shek, L.-Q. Xia;
DOI: 10.1109/IITC.2014.6831866 , Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC), 2014 IEEE International , pp. 185-188
San Jose California , **Invited Paper**.

134) "Ultrathin (8-14 nm) conformal SiN for sub-20 nm Copper/Low k interconnects" Son V. Nguyen, D. Priyadarshini, H. Shobha, T. Haigh Jr., C.-K. Hu, S. Cohen, E.Liniger, T. Shaw, E. Adams, J. Burnham, A. Madan, N. Klymko, C. Parks, D. Yang, , S. Moli*, G. Bonilla, A. Grill, D. Edelstein, D. Canaperi, L.-Q. Xia,S. Reiter, M. Balseanu, and M.Shek, May 12, Electrochemical Society Spring 2014 Meeting , Orlando, Florida. Published in ECS Transaction 2014: doi: 10.1149/06103.0017ecst *ECS Trans. 2014 volume 61, issue 3, pages 17-28*

135) "The development of lightly porous SiCOH dielectric films using plasma CVD with single OMCATS precursor chemistry " ; Deepika Priyadarshin, Hosadurga Shobha, Vince McGahay,Eric Liniger, Stehen A Cohen, Darryl Restaino, Thomas J Haigh Jr., Alfred Grill, Mark Sherwood; The New York State Center for Advanced Materials Processing Meeting , May 14-16, 2014 at Gideon Putnam Resort, Saratoga Springs, New York, USA. Invited Paper.

136) "Highly Reliable pSiCOH k=2.4 Interconnect Dielectric for Sub-10 nm Nodes Fabricated with Single Precursor" Son V. Nguyen, D. Priyadarshini, H. Shobha, T. Haigh Jr., C.-K. Hu, S. Cohen, E. Liniger, E. Adams, J. Burnham, J. Chen, H.

Huang, A. Madan, M. Shoudy, , T Shaw, E.T. ryan S. Molis, A. Grill, D. Canaperi, Material Research Society Spring 2015 Meeting, April 6-10,2015, San Francisco USA . **Invited Paper**.# BB04.1

137) "Selective Mn deposition for metal cap in nano Cu/pSiCOH low k interconnect." Son Nguyen, T. Vo, T. Haigh Jr., S. Cohen, P. Flaitz, T. Nogami, H. Shobha, D. Priyadarshini, Y. Lin, D. Canaperi, A. Grill, Roy Gordon, Y. Au . Atomic Layer Deposition Conference , July 2015, Portland Oregon

138) " Highly Robust Advanced Single Precursor Based k 2.4 ILD for Beol Cu Interconnects" D. Priyadarshini , S. V. Nguyen, H. K. Shobha , E. T. Ryan dries), S. M. Gates , H. Huang, J. Chen , E. Liniger, S. A. Cohen, C. K. Hu , A. Madan , E. Adams , S. E. Molis , T. J. Haigh , G. Bonilla , T. Standaert , D. F. Canaperi , and A. Grill . Electrochemical society Fall 2015 meeting. (Paper)
https://ecs.confex.com/ecs/228/webprogram/Paper58482.html

INTERNAL PUBLICATIONS

1) 30+ IBM Invention Disclosures published in IBM Technical Bulletin on various aspects in Material Sciences (Silicon Materials, Polymers, Adhesion, Structure and Properties Modification), Electronic Devices from 1983 to 1995.

2) About 50 Technical Reports on various aspects of Semiconductor and Computer Storage Technology (at IBM). One technical report on: "Coal Gasification and Kinetic Activity of Nickel Catalyst" (at Exxon).

US PATENTS:

Web External Link to Son Nguyen's patent list (partial list "incompleted" ~140 patents and applications on public record) :
http://patent.ipexl.com/inventor/Son_Van_Nguyen_1.html

More than 120+ Patents issued and filed to US Patent Office (120+ US Patents Issued)

1) APPARATUS FOR ACHIEVING ETCH RATE UNIFORMITY
US Patent 6051099 Issued 4/18/2000

2) REACTIVE ION ETCHING OF ALUMINA/TIC SUBSTRATES
Issued as US Patent 6001268, 12/14/1999

3) HIGH DENSITY PLASMA SURFACE MODIFICATION FOR IMPROVING ANTIWETTING PROPERTIES
US Patent # 6,132,813 Issued October 17, 2000

4) METHOD OF ETCHING CERAMICS OF ALUMINA/TIC WITH HIGH DENSITY PLASMA
Issued as US Patent# 6027660, 02/22/2000

5) LOW TEMPERATURE REFLOW DIELECTRIC FLUORINATED BPSG
US Patent # 6057350 Issued 05/02/2000

6) METHODS AND APPARATUS FOR FILLING HIGH ASPECT RATIO STRUCTURES WITH SILICATE GLASS

US Patent # 6077786 Issued 6/20/2000

7) FABRICATION METHOD FOR HIGH CAPACIANCE STORAGE NODE STRUCTURE
Issued as US Patent # 6027968 02/22/2000

8) FABRICATION METHOD FOR HIGH CAPACIANCE STORAGE NODE STRUCTURE
Issued as US Patent # 5753948 5/19/1998

9) SILICON ARTICLE HAVING COLUMNS AND METHOD OF MAKING
02/13/2001 Issued as Patent 6187412 in US

10) SILICON ARTICLE HAVING COLUMNS AND METHOD OF MAKING
12/03/2002 Issued as Patent 6489005 in US

11) INTEGRATED ULSI HEATSINK and Method of Making of
03/17/98 Issued as Patent 5729052 in US

12) INTEGRATED ULSI HEATSINK and Method of Making off
6/30/98 Issued as US Patent # 5773362

13) SHRINK-WRAP COLLAR FOR DRAM DEEP TRENCHES II ;
5/30/2000 ISSUED as US Patent # 6069049

14) IMPROVED METHOD FOR MAKING A PHOSPHOROUS DOPED CVD SILICON DIOXIDE THIN FILM
06/20/2000 Issued as US Patent #6077786

15) SEMICONDUCTOR DEVICE WITH HIGH DIELECTRIC CONSTANT INSULATOR MATERIAL

10/26/99 Issued as US Patent # 5973351

16) OXIDATION-RESISTANT SILICIDES FOR BARRIER LAYERS
Filed to US patent Office 6/4/97

17) APPARATUS AND METHOD FOR MAKING CVD FILMS
08/15/96 Filed as Docket FI996073 in US

18) SEMICONDUCTOR INSULATOR STRUCTURE USING MODULATION DOPED SILICATE GLASS

06/23/98 Issued as US Patent # 5770469

19) METHOD FOR SUPPRESSING PATTERN DISTORTION ASSOCIATED WITH BPSG REFLOW AND INTEGRATED CIRCUIT CHIP FORMED THEREBY
10/26/99 Issued as US Patent # 5973385

20) METHOD FOR SUPPRESSING PATTERN DISTORTION ASSOCIATED WITH BPSG REFLOW AND INTEGRATED CIRCUIT CHIP FORMED THEREBY
11/30/99 Issued as US Patent # 5994215

21) ADVANCED DAMASCENE PLANAR STACK CAPACITOR FABRICATION METHOD
05/19/98 Issued as Patent 5753948 in US

22) FLUORINE DOPED PLASMA ENHANCED PHOSPHO-SILICATE GLASS, AND
PROCESS. Issued as US Patent#5643640 , 7/01/97

23) Title: A LOW TEMPERATURE BPSG DEPOSITION PROCESS
01/11/2000 US Patent # 6013583

24) Title: LOW TEMPERATURE/LOW DOPANT OXIDE GLASS FILM
US Patent # 6489255 Issued 12/03/2002

25) Title: METHOD OF DEPOSITING FLUORINE DOPED OXIDE
10/08/96 Issued as Patent 5563105 in US

26) Title: HIGH DENSITY SELECTIVE Oxide:Nitride ETCHING USING A STOICHIOMETRICALLY ALTERED NITRIDE ETCH STOP.
US Patent # 5622596 issued April 22, 1997

27) Title: NON-RANDOM, SUB-LITHOGRAPHY VERTICAL STACK CAPACITOR
07/23/96 Issued as Patent 5538592 in US

28) Title: SHRINK-WRAP COLLAR FOR DRAM DEEP TRENCHES II
6/ 04/2002 Issued as US Patent #6399976

29 Title: ANGLE DEFINED TRENCH (ADT)
US patent number # 5610441 Issued March 11, 1997.

30) Title: ANGLE DEFINED TRENCH (ADT) ADVANCED STRUCTURE
09/30/97 Issued as Patent 5672537 in US

31) Title: TA205 THIN FILM BY LOW TEMPERATURE OZONE PLASMA ANNEALING (OXIDATION). Issued as US Patent# 5468687

32) Title: THIN CAPACITATOR DIELECTRIC BY RTP
Issued as US Patent# 5455204 in US

33) Method for Etching Boron Nitride
07/16/96 Issued as Patent 5536360 in US

34) Title: IMPROVED FLUORINATED SILICON NITRIDE FILMS
07/23/96 Issued as Patent 5539154 in US

35) Title: SELECTIVE ETCH PROCESS FOR BORON NITRIDE
Issued as US Patent# 5217567

36) Title: IMPROVED FLUORNIATED SILICON NITRIDE FILMS
Issued as US Patent# 5462812

37) Title: PLASMA CVD PROCESS FOR FLUORINATED SiN FILMS
Issued as US Patent# 5204138

38) European Patent # 94103684.0 : " Method for Etching Boron Nitride",
5/04/1994

39) Title: LOW TEMPERATURE PLASMA OXIDATION PROCESS FOR SIDEWALL SPACER
FORMATION- ENHANCEMENT. 05/02/95 Issued as US Patent# 5412246

40) Title: LOW TEMPERATURE PLASMA OXIDATION PROCESS FOR SIDEWALL SPACER FORMATION. Issued as US Patent# 5330935

41) Title:A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CELL
03/07/89 Issued as Patent 4811067 in US

42) Title: SELECTIVE DEPOSITION OF PARYLENE
07/10/96 Issued as Patent 2069078 in JA
02/03/98 Issued as Patents 5714798 in US

43) Title: SELECTIVE DEPOSITION OF PARYLENE - Process
04/08/97 Issued as Patent 5618379 in US

44)Title: METHOD FOR SUPPRESSING PATTERN DISTORTION ASSOCIATED WITH BPSG
REFLOW AND INTEGRATED CIRCUIT CHIP FORMED THEREBY. PART II.
US Patent # 5973385 , 10/26/1999

45)Title: SEMICONDUCTOR DEVICES STRUCTURE WITH HYDROGEN RICH LAYER FOR FACILITATING PASSIVATION OF SURFACE STATES

US Patent # 6483172, Issued November 19, 2002

46) Title: MAGNETIC RECORDING DEVICE HAVING AN IMPROVED SLIDER. US Patent # 6477011 Issued November 5, 2002

47) Title: " Flowable Spin-on Insulator", US Patent # 5855962 Issued January 5, 1999

48) Title : METHOD AND APPARATUS FOR IN-SITU MONITORING OF ION ENERGY DISTRIBUTION FOR ENDPOINT DETECTION VIA CAPACITANCE MEASUREMENT.. US Patent 6326794

49) " Storage System Slider Having Trailing Edge Pad and Method for making the same". US Patent # 6466408 Issued October 15, 2002

50): SELECTIVE AREA OXIDATION FOR PATTERNING MAGNETIC PERPENDICULAR CURRENT DEVICES, FILED to US Patent Office 5/2002

51): Process For Manufacturing a Magnetic Head Coil structure,
US Patent # 6901653 B2 Issued June 7, 2005.

52): APPARATUS FOR Patterning a SELF-ALIGNED COIL Using Damascene Process: US Patent# 7075750 Issued July 11, 2006

53): METHOD OF MANUFACTURING HIGH ASPECT RATIO PHOTOLITHOGRAPHIC FEATURES. Filed to US Patent Office 3/2001

54): CHEMICAL MECHANICAL POLISHING THICKNESS CONTROL IN MAGNETIC HEAD FABRICATION. -in US Patent #6776917 Issued 8/17/2004

55): PROCESSING OF MULTIPHASE CERAMIC SLIDER MATERIALS USING HARMONICALLY GENERATED ULTRAVIOLET LASER RADIATION. Filed to US Patent Office 11/1999

5&) METHOD OF DEPOSITING MATERIAL INTO HIGH ASPECT RATIO FEATURES USING ION BEAM DEPOSITION. US patent#6948231, 9/27/2005

58) Magnetic Transducer with a Write Head Having Multi-layer Coil.
US patent #7079355 B2 Issued July 18, 2006.
59) Method of Removing Magnetoresistive Sensor Cap by Reactive Ion Etching.
US Patent # 6919280 B2 Issued July 19, 2005
60) Current-In-Plane Magnetoresistive Sensor with Longtitudinal Biasing Layer having a nonmagnetic Oxide Central Region and Method for Fabrication of the sensor. Filed to US Patent Office 8/2002

Patents Issued and Filed from Applied Materials:
61) “Side Wall Passivation Films for Damascene Cu/Low K electronic Devices “, US Patent # 6878620 B2 Issued April 12, 2005
62) “ Modulated/Composited CVD low K films with Improved Mechanical and Electrical Properties for Nano electronic Devices” US Patent # 7011890 B2 Issued March 14, 2006
63) “Ultra Low K Plasma CVD Nanotube/Spin on Dielectrics with Improved Properties For Advanced Nanoelectronic Device Fabrication”, US Patent # 6984579 B2. Issued January 10, 2006.
64) “Method of Improving Interlayer Adhesion”,   US Patent # 6913992. Issued 07/05/2005;
65) “Method of Improving Interlayer Adhesion II”, US Patent # 7226876. Issued June 5, 2007
66) “Reacting an organosilicon compound with an oxidizing gas to form an ultra low k   dielectric” (pending). Filed to US Patent Office 4/2003
67) “Method of Forming low dielectric constant porous film “. US Patent # 7060638 Issued June 13, 2006

68) “ Method of Making a perpendicular Recording Magnetic Head Pole tip with an Etchable Adhesion CMP stop Layer” US Patent #7024756 Issued April 11, 2006
69) “A perpendicular Recording Magnetic Head with a Write Shield Magnetically Coupled to A first Pole Piece” , US Patent # 7031121 B2 Issued April 18, 2006
70) “Planarized Perpendicular Pole Tip System and Method for Manufacturing the same “ Filed to US Patent Office 7/2003
71) “Method for Patterning a Self-aligned Coil using a Damascene Process”

US Patent # 7022248 B2, Issued April 4, 2006

72)” Low k and Ultra Low K SiOH Dielectric Films and Methods to Form The Same ”, US patent # 7030468 Issued April 18, 2006

73) “Structure and Methods For integration of Ultra Low k Dielectrics with Improved Reliability”. US Patent#7088003. Issued 8/8/2006

74) “Method of Manufacturing a Current Perpendicular to-Plane Magneto resistive Devices with Oxidized Free Layer Side Regions, US Patent# 7043823 Issued May 16, 2006

75) “Hard mask for improved reliability of Silicon Based Dielectrics”

a) US Patent 7335980 issued 2/26/2008

76) “Hard mask for improved reliability of Silicon Based Dielectrics”

b) US Patent 7485582 B2 issued 2/3/2009

77) “Ultra low dielectric constant Layer with Controlled Biaxial Stress” , US patent 7357977 B2 issued 4/15/2008

78) “ SiCOH dielectric Material with Improved Toughness and Improve Si-C, Semiconductor Device Containing the same, and Method to make the same”

US Patent Patent 7479306 B2 issued 1/20/2009.

79) “Low k CVD Film Formation Process with in-situ Imbedded Nano Layers to improve Mechanical Properties”, Issued as Patent 7265437 in US Sept 4, 2007

80) “Advanced Low Dielectric Constant Organosilicon Plasma CVD Film” Son Nguyen et al. ,

a) US Patent # 7202564 issued 04/10/2007

81) “Advanced Low Dielectric Constant Organosilicon Plasma CVD Film” Son Nguyen ; US Patent # 7494938 B2 issued 2/24/2009

82)“IMPROVED SICOH DIELECTRIC”

01/20/2006 Filed to US Patent Office” . Co Inventors :Son Nguyen, Grill, A. Afzali-ardakani, A. Gates, S.M. Patel, V.V. , Neumayer, D.A.

83) “SICOH FILM PREPARATION USING PRECURSORS WITH BUILT-IN POROGEN FUNCTIONALITY”. US Patent # 7491658B2, Issued Feb 17, 2009

84) “SICOH FILM PREPARATION USING PRECURSORS WITH BUILT-IN POROGEN FUNCTIONALITY”.

and US Patent # 7521377 issued April 21, 2009

Co-inventors: Grill, A. Gates, S.M. Neumayer, D.A. Miller, R.D.

85) ENCLOSED NANOTUBE STRUCTURE AND METHOD FOR FORMING

US Patent # 7781267. Issued August 24 2010

86) “ METHOD FOR REDUCING FILM STRESS FOR SICOH LOW-K DIELECTRIC MATERIALS” US Patent # 7381659 Issued June 3, 2008

Co-inventors: Shaw, T.M.

87) “ MATERIALS CONTAINING VOIDS WITH VOID SIZE CONTROLLED ON THE NANOMETER SCALE “ US Patent # 7674521 , issued March 9, 2010

Co-inventors: Grill, A. Gates, S.M. Patel, V.V. Neumayer, D.A.

88) “ SICOH DIELECTRIC MATERIAL WITH IMPROVED TOUGHNESS AND IMPROVED SI-C BONDING, SEMICONDUCTOR DEVICE CONTAINING THE SAME, AND METHOD TO MAKE THE SAME” . US Patent # 7479306 Issued

January 20, 2009. US Patent Office. Co-inventors: Grill, A. Gates, S.M. Lane, M. Edelstein, D.C. Neumayer, D.A. Lin, Q. Miller, R.D. , A. Gates, S.M.

89) " AN IMPROVED METHOD FOR FABRICATING AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE "

a) US Patent # 7049247 issued May 23, 2006

90) " AN IMPROVED METHOD FOR FABRICATING AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE "

b) US Patent # 7312524 B2 Issued December 25, 2007

Co-inventors: Grill, A. Gates, S.M. Patel, V. Neumayer, D.A. Wang, X., Medeiros, D

.

91)" LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME" . US Patent 7282458 B2 issued 10/16/2007

92) Method of Improving The reliability of Magnetic Head Sensors by Ion Milling Smoothing. US Patent 6804878 Issued Oct 19, 2004

93) METHOD of FORMING LOW DIELECTRIC CONSTANT POROUS FILM US Patent # 7060638 Issued June 13, 2006

94) Method and Apparatus using a pre-patterned Seed Layer for providing an inductive head structure. US Patent # 7117583 Issued October 10, 2006

95) BEOL INTERCONNECT STRUCTURES WITH IMPROVED RESISTANCE TO STRESS, US Patent# 7847402 issued 12/07/2010.

96) EMBEDDED NANO UV BLOCKING BARRIER FOR IMPROVED RELIABILITY OF COPPER/ULTRA LOW K INTERLEVEL DIELECTRIC ELECTRONIC DEVICES, US patent # 7749892 Issued 7/21/2010

97) "Magnetic Head Coil Structure and Method for manufacturing the same" US Patent # 7304821 B2 Issued December 4, 2007.

98) "Method for manufacturing a magnetic head coil structure and/or pole tip structure".
US patent # 7313858 B2 issued January 1, 2008

99) "Advanced Multilayer Dielectric Cap with Improved Mechanical and Electrical Properties", US Patent#7737052, June 15, 2010.

100) "Magnetoresistive/Inductive write head assembly formed with seed layer having a uniformed thickness"
US Patent 7362543 B2 issued 4/22/2008

101) "Field Effect Transistor using carbon stress liner", US Patent# 7851288 , 12/14/2010.

102) Low k CVD Film Formation Process with in-situ Imbedded Nano Layers to improve Mechanical Properties. US Patent # 7998880. Issued 8/16/2011

103)" Method to modifying Interlayer Adhesion" , Son Van Nguyen, F.Schmitt, Li-Qun Xia, S.Venkatarama; US patent 7563728B2 , Issued July 21,2009

104)" Method to modifying Interlayer Adhesion" , Son Van Nguyen, F.Schmitt, Li-Qun Xia, S.Venkatarama; US patent 7960294 B2 , Issued June 21,2011

105) "ULTRA LOW K PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION PROCESSES USING A SINGLE BIFUNCTIONAL PRECURSOR CONTAINING BOTH A SICOH MATRIX FUNCTIONALITY AND ORGANIC POROGEN FUNCTIONALITY"
US Patent # 8097932, January 17, 2012

106) "METHOD OF FABRICATING A SICOH DIELECTRIC MATERIAL WITH IMPROVED TOUGHNESS AND IMPROVED SI-C BONDING". US Patent # 8101236; January 24, 2012

107) "AIR GAP INTERCONNECT STRUCTURES AND METHODS FOR FORMING THE SAME" , US Patent # 8120179, February 21, 2012

108) "ADVANCED LOW K CAP FILM FORMATION PROCESS FOR NANO ELECTRONIC DEVICES" Issued July 3, 2012. US Patent# 8212337 United States

109) " MATERIALS CONTAINING VOIDS WITH VOID SIZE CONTROLLED ON THE NANOMETER SCALE" Issued September 18, 2012 US Patent # 8268411

110) " Self-Aligned Composite M- MOx /dielectric Cap for Cu Interconnect structure" Issued Oct 30, 2012. US Patent # 8299365

Patents issue in 2013/2014

111)MULTI COMPONENT DIELECTRIC LAYER	2013-01-22	8357608	United States
112)ENGINEERED INTERCONNECT DIELECTRIC CAPS HAVING COMPRESSIVE STRESS AND INTERCONNECT STRUCTURES CONTAINING SAME	2013-01-29	8362596	United States
113) ENGINEERED INTERCONNECT DIELECTRIC CAPS HAVING COMPRESSIVE STRESS AND INTERCONNECT STRUCTURES CONTAINING SAME	2013-01-02	ZL201010227409.9	China

114) AIR GAP INTERCONNECT STRUCTURES AND METHODS FOR FORMING THE SAME	2013-02-26	8383507	United States
115) FORMATION OF AIR GAP WITH PROTECTION OF METAL LINES	2013-03-19	8399350	United States
116) THREE-DIMENSIONAL (3D) INTEGRATED CIRCUIT WITH ENHANCED COPPER-TO-COPPER BONDING	2013-04-30	8431436	United States
117) LOW K DIELECTRIC CVD FILM FORMATION PROCESS WITH IN-SITU IMBEDDED NANOLAYERS TO IMPROVE MECHANICAL PROPERTIES	2013-03-27	ZL200680007406.6	China
118) C-RICH CARBON BORON NITRIDE DIELECTRIC FILMS FOR USE IN ELECTRONIC DEVICES	2013-07-02	8476743	United States
119) SICOH DIELECTRIC MATERIAL WITH IMPROVED TOUGHNESS AND IMPROVED SI-C BONDING, SEMICONDUCTOR DEVICE CONTAINING THE SAME, AND METHOD TO MAKE THE SAME	2013-05-21	I397123	Taiwan
120) MULTILAYERED LOW K CAP WITH CONFORMAL GAP FILL AND UV STABLE COMPRESSIVE STRESS PROPERTIES	2013-07-23	8492880	United States

121)STRUCTURES AND METHODS FOR INTEGRATION OF ULTRALOW-K DIELECTRICS WITH IMPROVED RELIABILITY	2013-07-21	I402887	Taiwan
122)MULTILAYERED LOW K CAP WITH CONFORMAL GAP FILL AND UV STABLE COMPRESSIVE STRESS PROPERTIES	2013-09-17	8536069	United States
123)THREE-DIMENSIONAL (3D) INTEGRATED CIRCUIT WITH ENHANCED COPPER-TO-COPPER BONDING	2013-10-01	8546956	United States
124) LOW K DIELECTRIC CVD FILM FORMATION PROCESS WITH IN-SITU IMBEDDED NANOLAYERS TO IMPROVE MECHANICAL PROPERTIES	2013-11-01	5398258	Japan
125) MATERIALS CONTAINING VOIDS WITH VOID SIZE CONTROLLED ON THE NANOMETER SCALE	2013-12-31	8618183	United States
126)LOW K DIELECTRIC CVD FILM FORMATION PROCESS WITH IN-SITU IMBEDDED NANOLAYERS TO IMPROVE MECHANICAL PROPERTIES	2013-11-11	I414623	Taiwan
127) PROCESS TO FORM AN ADHESION LAYER AND MULTIPHASE ULTRA LOW K DIELECTRIC	2014-01-28	8637412	United States

MATERIAL USING PECVD			
128) C-RICH CARBON BORON NITRIDE DIELECTRIC FILMS FOR USE IN ELECTRONIC DEVICES	2014-02-18	8652950	United States
129)ADVANCED LOW K CAP FILM FORMATION PROCESS FOR NANO ELECTRONIC DEVICES	2014-03-04	8664109	United States
130) FORMATION OF AIR GAP WITH PROTECTION OF METAL LINES	2014-06-17	8754520	United States
131) INTERLEVEL DIELECTRICSTACK FOR INTERCONECT STRUCTURES	2014-07-15	8779600	United States
132) MULTILAYER DIELECTRIC STRUCTURES FOR SEMICONDUCTOR NANO-DEVICES	2015-03-17	8980715	United States
133) MULTILAYER DIELECTRIC STRUCTURES FOR SEMICONDUCTOR NANO-DEVICES	2015-03-17	8981466	United States
134) TITANIUM OXYNITRIDE HARD MASK FOR LITHOGRAPHIC PATTERNING	2015-03-24	8987133	United States
135) ADVANCED LOW K CAP FILM FORMATION PROCESS FOR NANO ELECTRONIC DEVICES	2015-05-26	9040411	United States
136)CORROSION/ETCHING PROTECTION IN INTEGRATION CIRCUIT FABRICATIONS	2015-06-09	9054109	United States
137) TITANIUM OXYNITRIDE HARD MASK FOR LITHO.	2015-07-21	9087876	United States

PATTERNING

138) (FDC)IMPROVED SICOH HARDMASK WITH GRADED TRANSITION LAYERS	2015-01-06	8927442	United States

Others International Patents (70+ Patents Issued)

Patent Tittles	Date Issued	Patent Number	Countries
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1989-11-16	586096	Australia
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1990-11-27	1277031	Canada
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	Switzerland
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	3772109708	Germany
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	Spain
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	France
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	United Kingdom
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	Italy

A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1995-09-27	1972276	Japan
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	Netherlands
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1991-08-14	248993	Sweden
A HIGH DENSITY VERTICALLY STRUCTURED 1 DEVICE DYNAMIC CEL	1989-03-07	4811067	United States
ADVANCED DAMASCENE PLANAR STACK CAPACITOR FABRICATION METHOD	2001-08-21	60130	Singapore
ANGLE DEFINED TRENCH (ADT)	2001-10-19	3242323	Japan
ANGLE DEFINED TRENCH (ADT)	1999-08-17	229573	Korea, Republic of
DOPED PEROVSKITE DIELECTRICS	2001-04-24	294998	Korea, Republic of
ETCH RATE ENHANCEMENT OF BN BY LOW CONCENTRATION SI DOPING	1997-06-20	2664866	Japan
ETCH RATE ENHANCEMENT OF BN BY LOW CONCENTRATION SI DOPING	1998-03-27	142150	Korea, Republic of
ETCH RATE ENHANCEMENT OF BN BY LOW CONCENTRATION SI DOPING	1995-06-07	NI-70034	Taiwan
GLASS FORMATION ON A SEMI-CONDUCTOR WAFER	2005-10-26	69832035.2	Germany

GLASS FORMATION ON A SEMI-CONDUCTOR WAFER	2005-10-26	0932188	United Kingdom
HIGH DENSITY SELECTIVE SIO2:SI3N4 ETCHING USING A STOICHIOMETRICALLY ALTERED NITRIDE ETCH STOP	2001-05-25	3193632	Japan
HIGH DENSITY SELECTIVE SIO2:SI3N4 ETCHING USING A STOICHIOMETRICALLY ALTERED NITRIDE ETCH STOP	1999-04-19	209041	Korea, Republic of
HIGH DENSITY SELECTIVE SIO2:SI3N4 ETCHING USING A STOICHIOMETRICALLY ALTERED NITRIDE ETCH STOP	1997-04-01	NI-85433	Taiwan
HIGH STABILITY PHOSPHOROUS DOPED FLOWABLE OXYNITRIDE SPIN ON GLASS	1999-08-20	2968244	Japan
LOW TEMPERATURE BPSG DEPOSITION PROCESS	2002-05-10	3304284	Japan
LOW TEMPERATURE PLASMA OXIDATION PROCESS FOR SIDEWALL SPACER FORMATION	1996-07-25	2075771	Japan
LOW TEMPERATURE REFLOW DIELECTRIC-FLUORINATED BPSG	2005-10-26	0932188	Ireland
LOW TEMPERATURE REFLOW DIELECTRIC-FLUORINATED BPSG	2005-10-26	0932188	Italy
LOW TEMPERATURE REFLOW DIELECTRIC-FLUORINATED BPSG	2001-06-01	3195299	Japan

LOW TEMPERATURE REFLOW DIELECTRIC-FLUORINATED BPSG	2002-10-30	360737	Korea, Republic of
LOW TEMPERATURE REFLOW DIELECTRIC-FLUORINATED BPSG	2005-10-26	0932188	Netherlands
DAMASCENE STACK CAPACITOR	2001-08-03	3217020	Japan
DAMASCENE STACK CAPACITOR	2001-04-18	NI-123770	Taiwan
DOPED PEROVSKITE DIELECTRICS	1999-05-21	2930569	Japan
METHOD FOR SUPPRESSING PATTERN DISTORTION ASSOCIATED WITH BPSG REFLOW AND INTEGRATED CIRCUIT CHIP FORMED THEREBY	2002-08-23	3342652	Japan
METHOD OF DEPOSITING FLUORINE DOPED OXIDE	2005-12-21	69534699.7	Germany
METHOD OF DEPOSITING FLUORINE DOPED OXIDE	2005-12-21	0704885	
METHOD OF DEPOSITING FLUORINE DOPED OXIDE	2005-12-21	0704885	France
METHOD OF DEPOSITING FLUORINE DOPED OXIDE	2005-12-21	0704885	United Kingdom
METHOD OF DEPOSITING FLUORINE DOPED OXIDE	2002-03-22	3290339	Japan
METHOD OF DEPOSITING FLUORINE DOPED OXIDE	1996-10-09	NI-78762	Taiwan

NON-RANDOM, SUB-LITHOGRAPHY VERTICAL STACK CAPACITOR	2000-07-07	3086403	Japan
NON-RANDOM, SUB-LITHOGRAPHY VERTICAL STACK CAPACITOR	1998-07-29	157350	Korea, Republic of
NON-RANDOM, SUB-LITHOGRAPHY VERTICAL STACK CAPACITOR	1998-04-09	NI-91409	Taiwan
SELECTIVE DEPOSITION OF PARYLENE	1996-07-10	2069078	Japan
TA205 THIN FILM BY LOW TEMPERATURE OZONE PLASMA ANNEALING (OXIDATION)	2001-06-22	3202893	Japan
LOW TEMPERATURE REFLOW DIELECTRIC-FLUORINATED BPSG	2000-11-01	NI-122675	Taiwan
METHODS TO FORM SICOH OR SICNH DIELECTRICS AND STRUCTURES INCLUDING THE SAME	2009-10-21	ZL200710126919.5	China
HARDMASK FOR IMPROVED RELIABILITY OF SILICON BASED DIELECTRICS	2008-05-14	ZL200510117378.0	China
LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME	2008-04-02	ZL200510004304.6	China
(E-DOCKET)ENCLOSED NANOTUBE STRUCTURE AND METHOD FOR FORMING	2009-02-11	ZL200710102309.1	China
STRUCTURES AND METHODS FOR	2009-06-19	4328725	Japan

INTEGRATION OF ULTRALOW-K DIELECTRICS WITH IMPROVED RELIABILITY			
AN IMPROVED METHOD FOR FABRICATING AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE	2009-08-05	ZL200580011628.0	China
SICOH DIELECTRIC MATERIAL WITH IMPROVED TOUGHNESS AND IMPROVED SI-C BONDING, SEMICONDUCTOR DEVICE CONTAINING THE SAME, AND METHOD TO MAKE THE SAME	2009-09-09	ZL200610002175.1	China
ADVANCED LOW DIELECTRIC CONSTANT ORGANOSILICON PLASMA CHEMICAL VAPOR DEPOSITION FILMS	2009-08-26	ZL200680004568.4	China
ULTRA LOW K PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION PROCESSES USING A SINGLE BIFUNCTIONAL PRECURSOR CONTAINING BOTH A SICOH MATRIX FUNCTIONALITY AND ORGANIC POROGEN FUNCTIONALITY	2009-10-21	ZL200510112743.9	China
AN IMPROVED METHOD FOR FABRICATING AN	2010-04-29	956580	Korea, Republic of

ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE			
LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME	2010-05-01	I324381	Taiwan
IMPROVED SICOH DIELECTRIC	2010-07-21	ZL200710002003.9	China
GLASS FORMATION ON A SEMI-CONDUCTOR WAFER	2005-10-26	0932188	France
DEVICE STRUCTURE WITH LAYER FOR FACILITATING PASSIVATION OF SURFACE STATES	2006-09-29	633191	Korea, Republic of
DEVICE STRUCTURE WITH LAYER FOR FACILITATING PASSIVATION OF SURFACE STATES	2002-02-08	NI-142691	Taiwan
DEVICE STRUCTURE WITH LAYER FOR FACILITATING PASSIVATION OF SURFACE STATES	2004-10-13	ZL99103121.0	China
ADVANCED LOW DIELECTRIC CONSTANT ORGANOSILICON PLASMA CHEMICAL VAPOR DEPOSITION FILMS	2010-11-30	998809	Korea, Republic of
LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME	2011-06-03	4755831	Japan

AN IMPROVED METHOD FOR FABRICATING AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE	2011-06-03	4756036	Japan
DOPED PEROVSKITE DIELECTRICS	1999-03-11	NI-097787	Taiwan
ADVANCED LOW DIELECTRIC CONSTANT ORGANOSILICON PLASMA CHEMICAL VAPOR DEPOSITION FILMS	2011-08-11	I346982	Taiwan
EMBEDDED NANO UV BLOCKING BARRIER FOR IMPROVED RELIABILITY OF COPPER/ULTRA LOW K INTERLEVEL DIELECTRIC ELECTRONIC DEVICES	2011-09-21	ZL200710186782.2	China
LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME	2011-09-30	4833268	JAPAN
LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME	2011-06-03	4755831	Japan
AN IMPROVED METHOD FOR FABRICATING AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR	2011-06-03	4756036	Japan

DEVICE AND ELECTRONIC DEVICE MADE			
DOPED PEROVSKITE DIELECTRICS	1999-03-11	NI-097787	Taiwan
ADVANCED LOW DIELECTRIC CONSTANT ORGANOSILICON PLASMA CHEMICAL VAPOR DEPOSITION FILMS	2011-08-11	I346982	Taiwan
EMBEDDED NANO UV BLOCKING BARRIER FOR IMPROVED RELIABILITY OF COPPER/ULTRA LOW K INTERLEVEL DIELECTRIC ELECTRONIC DEVICES	2011-09-21	ZL200710186782.2	China
LOW K AND ULTRA LOW K SICOH DIELECTRIC FILMS AND METHODS TO FORM THE SAME	2011-09-30	4833268	Japan
AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE	2011-12-01	I353637	Taiwan
ULTRALOW DIELECTRIC CONSTANT LAYER WITH CONTROLLED BIAXIAL STRESS	2012-08-17	5065054	Japan
(E-DOCKET)ENCLOSED NANOTUBE STRUCTURE AND METHOD FOR FORMING	2012-08-24	5068100	Japan
ULTRALOW DIELECTRIC	2012-10-03	ZL200680002276.7	China

CONSTANT LAYER WITH CONTROLLED BIAXIAL STRESS			
DIELECTRIC CAP HAVING MATERIAL WITH OPTICAL BAND GAP TO SUBSTANTIALLY BLOCK UV RADIATION DURING CURING TREATMENT, AND RELATED METHODS	2012-09-05	ZL200880001994.1	China
AN IMPROVED METHOD FOR FABRICATING AN ULTRALOW DIELECTRIC CONSTANT MATERIAL AS AN INTRALEVEL OR INTERLEVEL DIELECTRIC IN A SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE MADE	2012-10-11	I374472	Taiwan
ALBANY-ENGINEERED INTERCONNECT DIELECTRIC CAPS HAVING COMPRESSIVE STRESS AND INTERCONNECT STRUCTURES CONTAINING SAME	2013-01-02	ZL201010227409.9	China
LOW K DIELECTRIC CVD FILM FORMATION PROCESS WITH IN-SITU IMBEDDED NANOLAYERS TO IMPROVE MECHANICAL PROPERTIES	2013-03-27	ZL200680007406.6	China
SICOH DIELECTRIC MATERIAL WITH IMPROVED TOUGHNESS AND IMPROVED SI-C BONDING, SEMICONDUCTOR DEVICE CONTAINING THE SAME, AND	2013-05-21	I397123	Taiwan

METHOD TO MAKE THE SAME			
STRUCTURES AND METHODS FOR INTEGRATION OF ULTRALOW-K DIELECTRICS WITH IMPROVED RELIABILITY	2013-07-21	I402887	Taiwan
LOW K DIELECTRIC CVD FILM FORMATION PROCESS WITH IN-SITU IMBEDDED NANOLAYERS TO IMPROVE MECHANICAL PROPERTIES	2013-11-01	5398258	Japan
LOW K DIELECTRIC CVD FILM FORMATION PROCESS WITH IN-SITU IMBEDDED NANOLAYERS TO IMPROVE MECHANICAL PROPERTIES	2013-11-11	I414623	Taiwan
ADVANCED LOW DIELECTRIC CONSTANT ORGANOSILICON PLASMA CHEMICAL VAPOR DEPOSITION FILMS	2014-01-31	5466365	Japan
DIELECTRIC CAP HAVING MATERIAL WITH OPTICAL BAND GAP TO SUBSTANTIALLY BLOCK UV RADIATION DURING CURING TREATMENT, AND RELATED METHODS	2015-01-16	5679662	Japan

PROFESSIONAL ASSOCIATIONS and Other Scientific and Academic Activities

- Electrochemical Society
- American Chemical Society
- Material Research Society
- International Union of Pure and Applied Chemistry
- Senior Member of US Committee for Scientific Cooperation with Viet Nam (Active Senior Member) since 1978 helping 100+ of Vietnamese graduate students scientist visit and obtain educational opportunities in USA.
- Academic Advisor for Tra Vinh University, Vietnam. Chemical and Nanoscience Program since 2006
- Technical Science Advisor for Material Science Program, Vietnam National University, Ho Chi Minh City, Vietnam , appointed 2008-2013.

REFERENCES –

1) Jeffrey Gambino, Ph.D.
   Senior Technical Staff Member
   IBM Essex Junction, Vermont USA
   Phone: 1-802-769-0433 ; Cell Phone : 1-802-316-0342
   E-mail: Gambinoj@us.ibm.com
2) Professor Walter Varhue,
   Department of Electrical Engineering, University of Vermont,
   Phone: 1-802-656-8505,
   E-mail:varhue@emba.uvm.edu